UNIVERSITY OF RUHUNA

BACHELOR OF SCIENCE SPECIAL DEGREE LEVEL I (Semester II) EXAMINATION OCTOBER- 2021

Subject: PHYSICS
Course unit: PHY4112, Electronics II **TIME: 02 hours**

No. of Questions: Five (05) **No. of Pages: Three (03)**

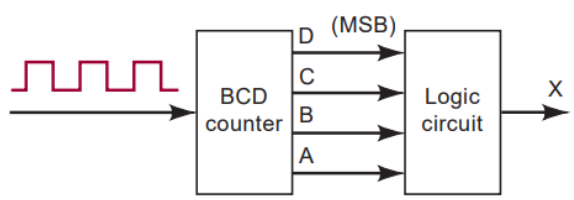
Answer FOUR (04) questions only

Q1.

a) In digital imaging, a pixel is the smallest item of information in an image, where more pixels typically provide more accurate representations of the original. A 3-Megapixel digital camera stores an eight-bit number for each primary colour (red, green, blue) found in each picture element (pixel). If every bit is stored, how many pictures can be stored on a 128-Megabyte memory card? (Note: In binary, Mega means 2^{20})

[03 marks]

b) The BCD counter shown in the figure produces a four-bit output representing the BCD code for the number of pulses that have been applied to the counter input.



i. Write down the possible counting range in binary form for this counter.

ii. Design the logic circuit using two ANDs, one OR, and one NOT gate that produces X = 1 whenever the count is 2, 3, or 9. Use K mapping and take advantage of the don't care conditions.

[10 marks]

c) The movement of binary data and codes from one location to another is the most frequent operation performed in a digital system.

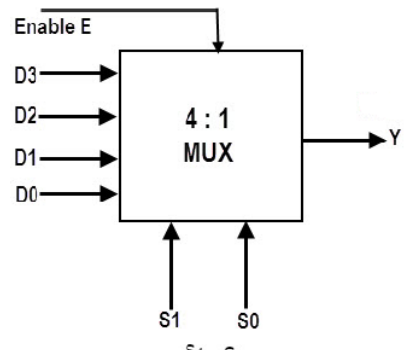
i. What is the major cause of the error, and why is it significant in the transmission process?

ii. Briefly discuss the parity method in detecting an error code.

iii. In the parity method, what is the mechanism use to identify a corrupted bit of a code word.

[12 marks]

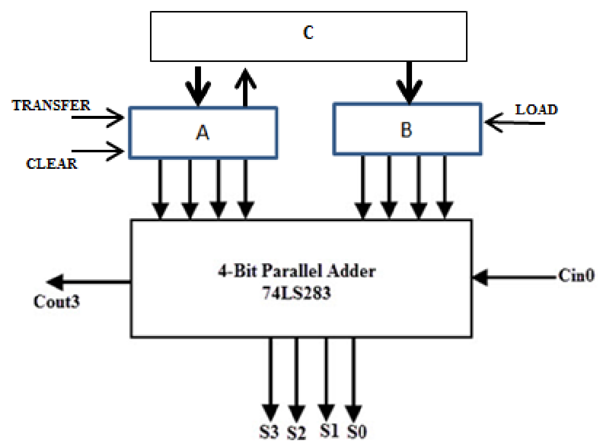
Q2. MSI components perform specific digital functions commonly needed in the design of digital systems. The multiplexer is a versatile application of MSI logic circuits. The logic symbol of a MUX is shown in the figure.



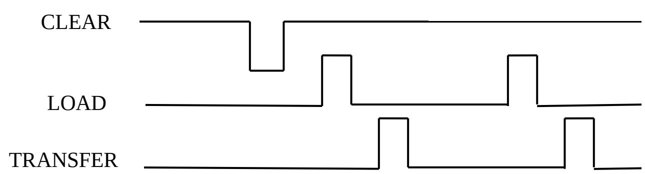
i. What does a multiplexer do?
ii. Considering all inputs and output, discuss the operation of the multiplexer shown in the diagram.
iii. Using AND, OR, and INVERTER gate combinations, design and draw the circuit diagram of 4 to1 multiplexer.
iv. You are provided with only a dual 4 to1 Multiplexer chip and a quad Inverter chip. Design and draw the circuit diagram for a one-bit full adder circuit by using the given chips appropriately.

[25 marks]

Q3. Several parallel adders are available as ICs. The most common is the four-bit parallel adder, illustrated in the figure. All the bits of A and B are fed into the adder circuits simultaneously, and therefore parallel addition is speedy.



i. What are the A, B, and C circuits of the given adder circuit?
ii. Write down the complete adder's operation sequence by following the given timing diagram for adding two binary numbers 1001 and 0101.

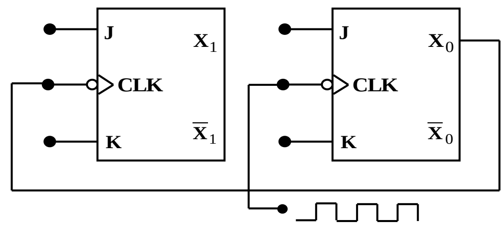


iii. What is the main cause for the delay of operation in an adder circuit, and what remedy has been used in this circuit to overcome the delay?
iv. Redraw the circuit diagram with necessary modifications to perform **both addition and subtraction** operations.
v. Determine outputs of the circuit in part iv, in both operations when ADD is on and SUB is on for the following BCD inputs A=[0111] and B=[0110].

[25 marks]

Q4.

Clocked flip-flops are versatile devices that can be used in various applications, including frequency division and counting. The figure shows the wiring arrangement of two J-K flip-flops to form a two-bit binary counter.



a)

i. Extend the flip-flop arrangement for a 3-bit asynchronous (ripple) up counter.

ii. Modify the same counter to perform the counting operations only between 2 and 5.

[10 marks]

b)

i. Discuss the significant drawback of ripple counters and give a possible mechanism to overcome this drawback.

ii. Design and draw the logic circuit diagram of the 3-bit synchronous up counter.

iii. Draw the circuit diagram of a 3-bit ring counter and write down its entire operation cycle by considering the initial outputs to be 100).

[15 marks]

Q5.

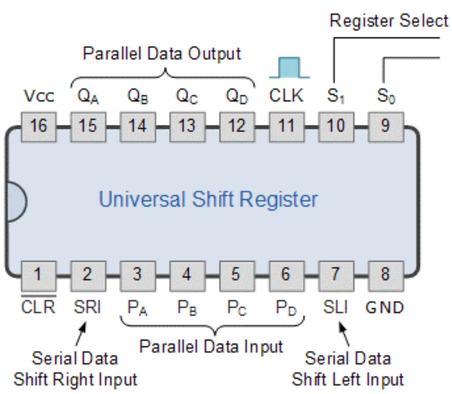
a) Discuss the following Flip-Flop applications.

i. Flop-Flop synchronizations.

ii. Detecting the input sequence.

[10 marks]

b) A register is formed by combining a group of flip-flops used to store a binary word. Pin arrangement of a universal shift register is shown in the figure.



i. What are the uses of pins 8 & 16?

ii. What are the uses of pins 1 & 11?

iii. Briefly discuss the uses of pins 9 & 10 with their possible combinations.

iv. Stating the relevant PINs discuss the following operations of the universal shift register. Give at least one application for each.

a. SISO

b. SIPO

c. PIPO

d. PISO

[15 marks]