UNIVERSITY OF RUHUNA

BACHELOR OF SCIENCE SPECIAL DEGREE LEVEL I/II (Semester II)
EXAMINATION DECEMBER- 2020

Subject: PHYSICS
Course unit: PHY4112, Electronics II **TIME: 02 hours**

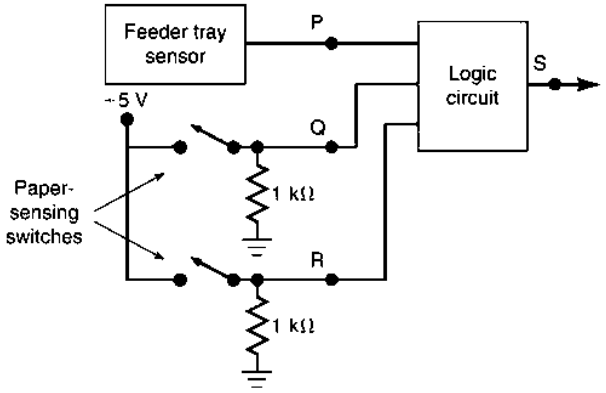
Answer FOUR (04) questions only

Q1.

a) A 32-bit computer uses hexadecimal codes to represent its memory addresses.
   i. How many hex digits are required?
   ii. What is the range of addresses in hex?
   iii. How many memory locations are there?

[06 marks]

b) As illustrated in the figure, in a simple photo copy machine, a stop signal, S, is to be generated to stop the machine operation and energize an indicator light whenever either of the following conditions exists:
   1. there is no paper in the paper feeder tray; or
   2. the two micro switches in the paper path are activated, indicating a jam in the paper path.



The presence of paper in the feeder tray is indicated by a HIGH at logic signal P. Each of the micro switches produces a logic signal (Q and R) that goes HIGH whenever paper is jammed over the switch to activate it.

Design a logic circuit to produce a HIGH at output signal S for the stated conditions.

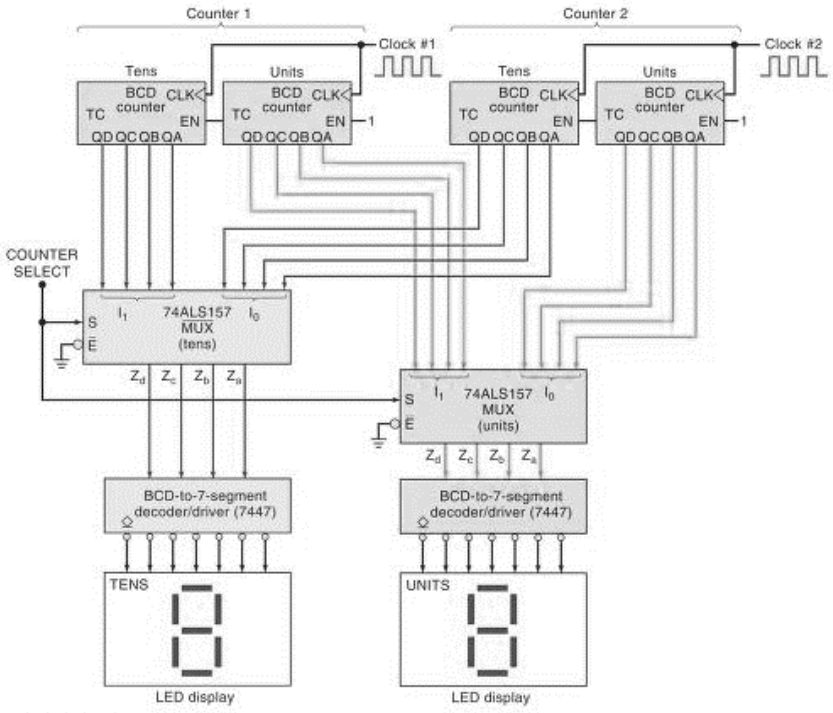
[10 marks]

c) Briefly discuss the parity method in detecting the error code.

[09 marks]

Q2.

Digital systems obtain binary coded data and information that are continuously being operated on in some manner like decoding and encoding, multiplexing and demultiplexing etc. Figure shows a circuitry contains in a digital clock for displaying two multidigit BCD counters one at a time.



a) Give a short description on functioning of the circuit.

[07 marks]

b)

i. What is the purpose of use of decoder drivers in the circuit?

ii. Complete the truth table for 2 -to- 4-line decoder (active low) with an ENABLE input.

iii. Implement the decoder driver using relevant gates.

[09 marks]

c)

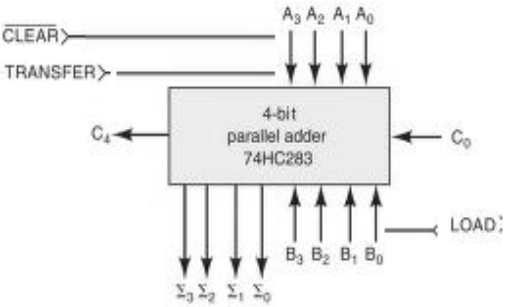
i. What is the use of multiplexers in the circuit?

ii. Giving the logic function draw the circuit diagram of two-input multiplexer using relevant gates.

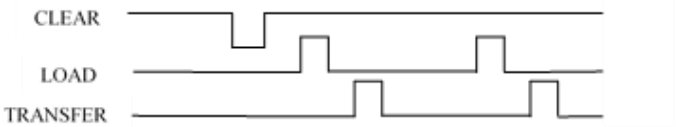
[09 marks]

Q3.

Figure shows the functional symbol for the 74HC283 four-bit parallel adder. Three commands used in operation are also shown in the figure.



a) Write down the sequence of operation of the complete adder by following the given timing diagram.



[06 marks]

b) Add 59 and 38 in BCD.
Extend the adder circuit to accomplish above addition (in part ii) by cascading two 74HC283 ICs.

[08 marks]

c) Subtract 4 from 9 using 2's compliment system.
Modify the given adder (74HC283) to perform the subtraction operation.

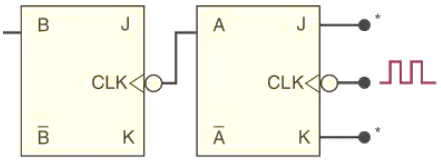
[08 marks]

d) What is the main cause of the delay in a parallel adder circuit and what remedy has been used in this circuit to overcome the delay?

[03 marks]

Q4.

Figure shows a two-bit asynchronous counter circuit composed of two J-K flip-flops.



a)

i. Extend the given circuit for 3-bit asynchronous counter.

ii. What are up counters and down counters and what changes has to be taken to convert this circuit to down counter?

iii. By drawing all waveforms explain the operation of 3-bit up counter. Write down the sequence of counting operations.

iv. Modify the same counter circuit to perform the counting operations between 2 and 5.

[18 marks]

b) Design a logic circuit for 3-bit **synchronous up** counter.

[07 marks]

Q5.

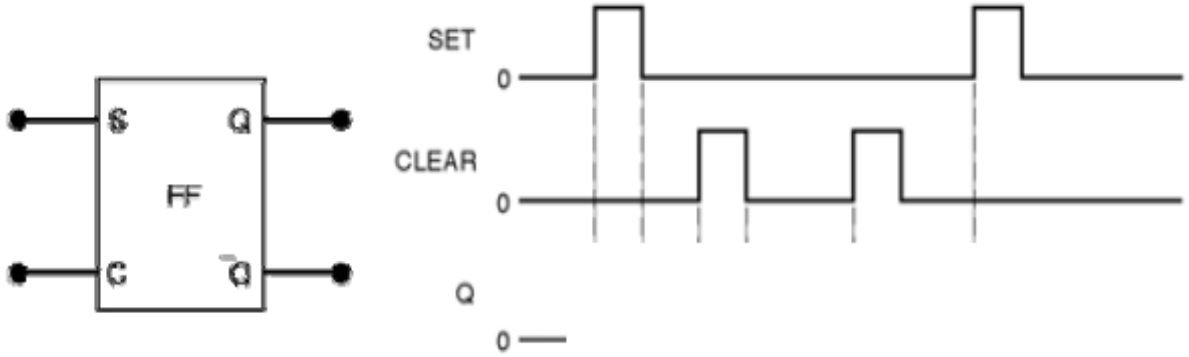
a) Discuss **any two** of followings relating to Flip-Flops.

i. Flop-Flop synchronizations
ii. Detecting the input sequence
iii. Setup and Hold times

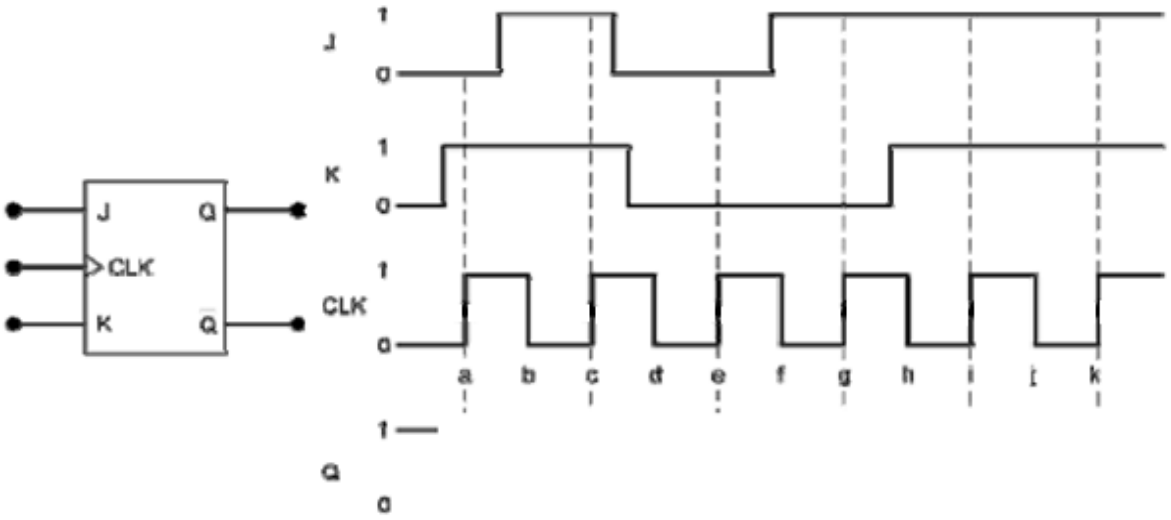
[10 marks]

b) Use the same sheet to answer this question and attached with your answer scripts. Complete the output wave forms of given flip-flops (i to v) according to their inputs.

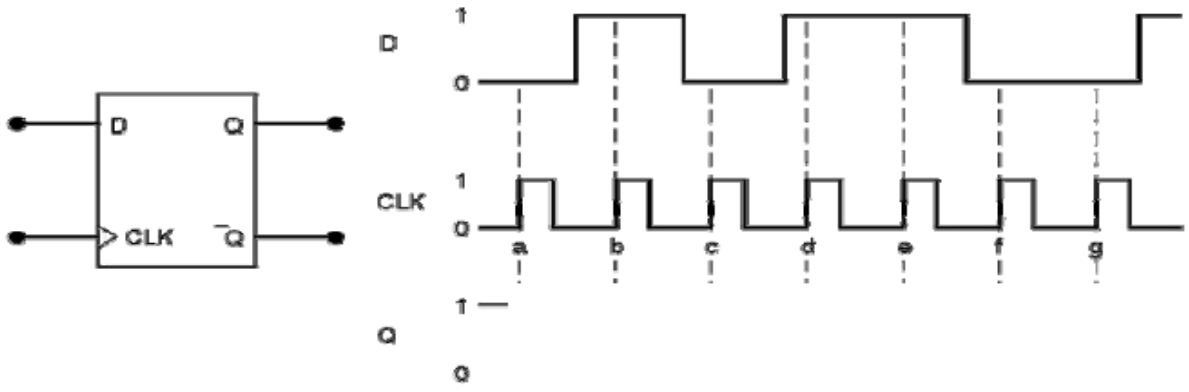
i.



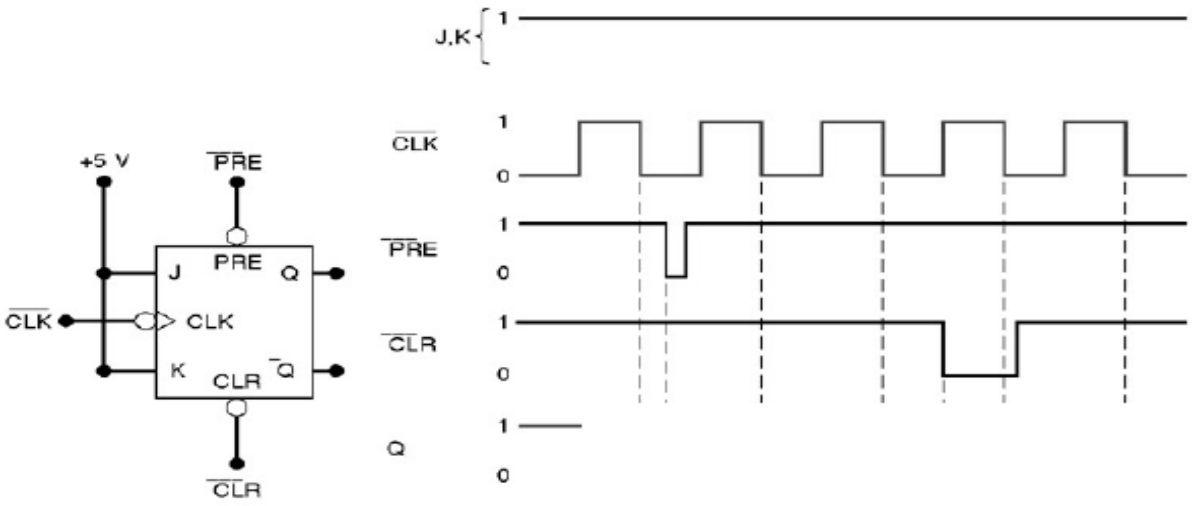
ii.



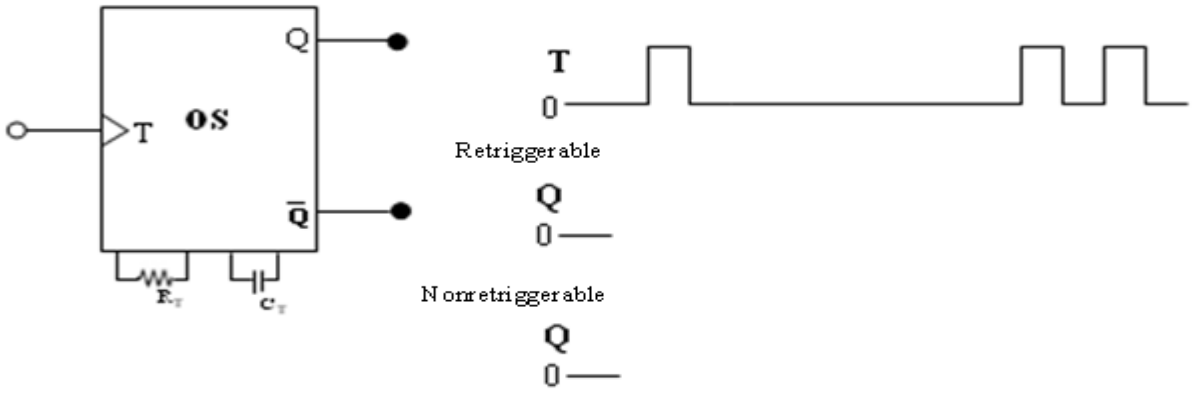
iii



iv



v



(Note: Quasi stable interval is 2 ms (> width of the clock pulse) for **both cases)**

[15 marks]