UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 7 Examination in Engineering: August 2015

Module Number: EE7235 **Module Name: Power Electronic Applications**

[Three Hours]

[Answer all questions, each question carry 10 marks]

Q1   a)   In conventional switching mode power supplies, the switching elements in an inverter leg turn-on and turn-off alternatively during each switching period. Therefore, the switching losses increase with switching frequency. One popular method is to use resonant techniques to force the switching devices to turn-on and turn-off at zero current or zero voltage to reduce the switching losses.

   i)   Draw a switch-mode inverter leg and briefly explain the operation of a controllable switch using typical waveforms of voltage, current and power through a controllable switch during turn-off and turn-on.

   ii)   Using the waveforms you have drawn in i), briefly explain the drawbacks associated with switch-mode operation of converters.

[3 Marks]

   b)   In order to overcome the drawbacks mentioned in part a) ii), a step down DC-DC converter can be modified using a simple LC resonant circuit based on the parallel resonant circuit concept as shown in Figure Q1.

   i)   Draw the current waveform through the resonant inductor and the voltage waveform across the resonant capacitor for one switching cycle. (**The answers without supporting reasons and calculations will not carry marks**)

   Note:
   The current through the resonant inductor and the voltage across the resonant capacitor for a parallel resonant circuit is given by following expressions with their usual notations.

$$i_{L_r}(t) = I_d + (I_{LO} - I_d)\cos[\omega_0(t - t_0)] + \frac{V_{co}}{Z_0}\sin[\omega_0(t - t_0)]$$

$$v_{C_r}(t) = Z_0(I_d - I_{LO})\sin[\omega_0(t - t_0)] + V_{co}\cos[\omega_0(t - t_0)]$$

   ii)   Calculate the characteristic impedance (Z_0) value and the maximum current through the resonant inductor for the given values in Figure Q1.

[7.0 Marks]

Q2 a) Figure Q2 shows the circuit diagram of a step down DC-DC converter which converts 12 V supply voltage to 1.5 V output voltage. The current drawn by the load is 20 A.

i) Modify the circuit shown in Figure Q2 to achieve the Zero Voltage Switching (ZVS) using the series resonant circuit concept.

ii) Draw the waveform of the current through the resonant inductor and the waveform of the voltage across the resonant capacitor for one switching cycle.

iii) Derive expressions for $i_{L_r}(t)$ and $v_{C_r}(t)$ while the circuit drawn in i) is working as a series resonant circuit.

Note:
The current through the resonant inductor and the voltage across the resonant capacitor for a series resonant circuit is given by following expressions with their usual notations.

$$i_{L_r}(t) = I_{LO}\cos[\omega_0(t - t_0)] + \frac{V_d - V_{co}}{Z_o}\sin[\omega_0(t - t_0)]$$

$$v_{C_r}(t) = V_d - (V_d - V_{co})\cos[\omega_0(t - t_0)] + I_{LO}Z_o\sin[\omega_0(t - t_0)]$$

iv) Using the expressions derived in iii), calculate the maximum and minimum voltage and current values (if necessary, in terms of characteristic impedance (Z_o)) with relevant time periods. Mark the obtained voltage and current values on the waveform drawn in ii).

[5.5 Marks]

b) To design the modified step down DC-DC converter in part a) i) with 118 kHz resonant frequency, L_r and C_r must satisfy the sufficient condition for natural turn off of the switch at zero voltage.

i) State the condition for natural turn off of ZVS.

ii) Show that $L_r > \dfrac{V_d}{\omega_0 I_o}$ and $C_r < \dfrac{I_o}{\omega_0 V_d}$ for the natural turn off.

Note:
All symbols carry their usual meanings.

iii) Calculate the minimum L_r and maximum C_r values for the design considerations in order to satisfy condition in i).

[4.5 Marks]

Q3 a) Nonlinear loads such as power electronic loads generate harmonic currents and voltages in the utility grid.

i) Explain how the voltage at the Point of Common Coupling (PCC) of utility grid is distorted due to harmonic currents generated by power electronic loads using a suitable diagram and expressions.

ii) Derive an expression for the percentage harmonic distortion (%V_h) using the diagram drawn in i).

iii) Explain the variation of harmonic order h with the ratio of I_h/I_1 and with the ratio of I_{sc}/I_1 for a fixed harmonic voltage distortion.

[3.5 Marks]

b) Harmonic current distortion is shown in Table Q3.

   i) What is the basic idea of IEEE - 519 standard?

   ii) Due to a nonlinear load connected to a system, it has the maximum short circuit current I_{sc}= 2.2 kA. Check whether the limitations in Table Q3 are satisfied, if the rms current drawn from the source (I_s) is 100 A and resulting harmonic components are $I_3 = 4$ A, $I_7 = 2.5$ A, $I_9 = 0.9$ A, $I_{13} = 0.5$ A and $I_{15} = 0.2$ A.

[3 Marks]

c) i) Briefly explain the following harmonic problems arise due to the nonlinear loads in a power system.

    I) The system power factor is reduced and increased the utility cost.

    II) The sensitive devices are not properly working in power systems.

   ii) List 3 different harmonic reduction methods applied in electrical systems and briefly explain the principle of active filtering.

[3.5 Marks]

Q4 a) Power electronic converters become Electromagnetic Interference (EMI) sources due to their fast switching operations.

   i) What is meant by EMI?

   ii) Briefly explain two types of conducted EMI with the help of relevant diagrams.

   iii) Name the methods used to reduce the EMI.

[2.5 Marks]

b) i) Draw a schematic diagram to illustrate the circuit configuration of a three phase to three phase matrix converter.

   ii) What are the requirements and restrictions on the operation of matrix converters?

   iii) Discuss the pros and cons of the matrix converter.

[2.5 Marks]

c) i) Explain why a HVDC system is economically justifiable for power transmission, only beyond a certain threshold transmission distance.

   ii) With the help of a schematic diagram discuss about the major components of a HVDC converter station.

   iii) Explain the reason for having a special transformer arrangement in the HVDC system.

   iv) Explain why 12 pulse line-frequency converters are preferred over 6 pulse line-frequency converters for power conversion in HVDC transmission.

[5 Marks]

Q5 Figure Q5 shows a circuit diagram of a forward converter.

a) Assuming the complete demagnetizing of the core, draw the waveforms of V_1, i_m, i_3, i_1 and i_L for one switching cycle.

[2.5 Marks]

b) The forward converter shown Figure Q5 is connected to 230 V, 50 Hz utility grid via a diode rectifier. The following data is given for the forward converter.

$f_s = 80$ kHz (switching frequency of the forward converter)
$L_0 = 25$ μH
$R_0 = 4 \, \Omega$
$N_1: N_2: N_3 = 230 :10 :115$

The output capacitor of the diode rectifier and output capacitor in the forward converter are sufficiently large to justify the assumption of V_d and V_0 being constant.

The forward converter is lossless and can operate in both continuous and discontinuous conduction mode.

i) Describe the function of the third winding.

ii) Calculate output voltage of the diode rectifier bridge.

iii) Calculate the allowable control range of the duty ratio D.

iv) What values can the output voltage take when the duty ratio is varied over the allowable control range, if the converter operates in continuous conduction mode?

v) Calculate D, for an output voltage of 5 V.

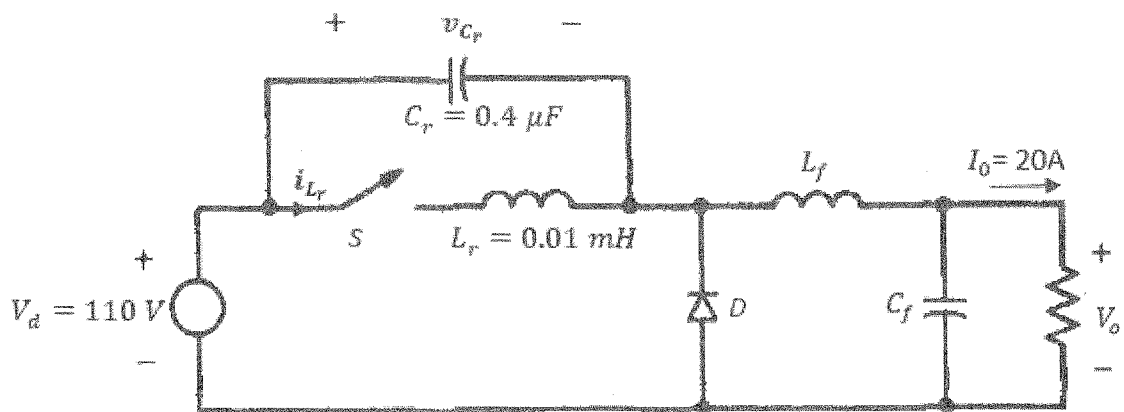vi) Calculate the input power for the operating condition in part v).

[7.5 Mark]
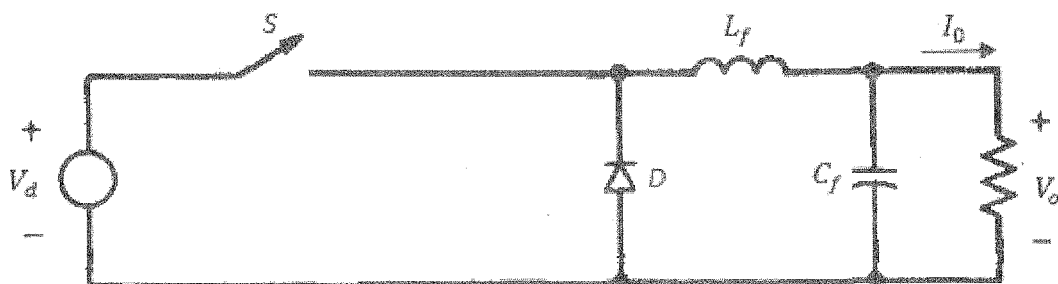

Figure Q1 : ZCS step down DC-DC converter

Figure Q2 : Step down DC-DC converter

Table Q3 : Harmonic current distortion I_h/I_1

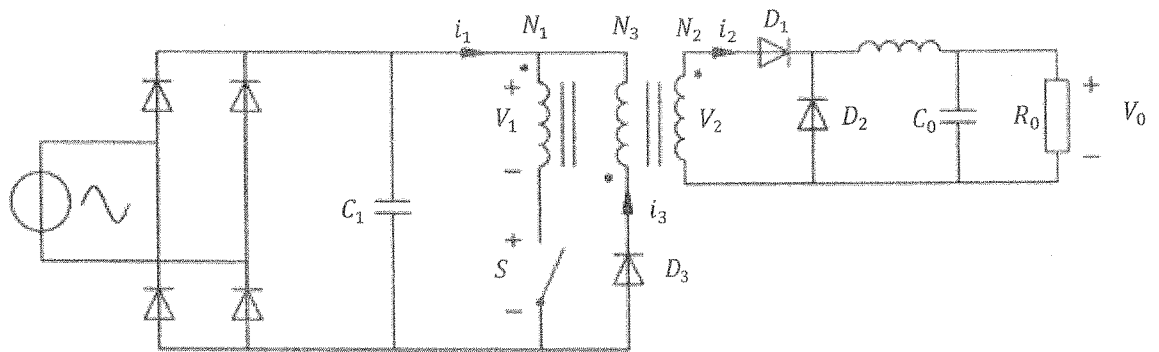| I_{SC}/I_1	Odd Harmonic Order h (%)					Total Harmonic Distortion (%)
	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	
<20	4.0	2.0	1.5	0.6	0.3	5.0
20–50	7.0	3.5	2.5	1.0	0.5	8.0
50–100	10.0	4.5	4.0	1.5	0.7	12.0
100–1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Figure Q5 : Forward Converter