UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5 Examination in Engineering: March 2022

Module Number: EE5201 **Module Name: Computer Architecture**

[Three Hours]

[Answer **all questions**, each question carries 12.5 marks]

Q1 a) Instruction pipelining is used for improving the performance of microprocessors. List three other techniques built into processors for improving the performance.

[1.5 Marks]

b) Briefly explain the following.

i) Many integrated core processors.

[1 Mark]

ii) Instruction cycle with interrupts.

[1 Mark]

iii) Point-to-Point interconnect.

[1 Mark]

c) Certain properties of the instruction set of the IAS computer are given in Table Q1. Calculate the performance of the instruction set with respect to an appropriate performance parameter.

[3 Marks]

d) i) Suppose that a program consists of 40% instructions that can be parallelized and the program run on a quad-core processor. Calculate the "Speedup" of the program.

[2 Marks]

ii) Suppose that the instruction set given in Table Q1 is to be used along with the same quad-core processor. The program written, using the instructions, consists of 10% branch instructions, 10% address modify instructions, and equal percentages of the arithmetic and data transfer instructions. Calculate the speedup of the program, showing all your calculations.

[3 Marks]

Q2 a) Von Neumann's stored program computer was introduced in 1946. Its architecture is given in Figure Q2.

i) Identify three main structural components of computers built using Von Neumann architecture.

[1.5 Marks]

ii) State the meaning of the term "Stored program concept".

[1 Mark]

iii) Word size of this architecture is 40 bits and words are of two types. State how the words are constructed.

[2 Marks]

iv) Briefly explain how Fetch and Execute cycles are performed in this machine, mentioning the specific registers used in the process.

[3 Marks]

b) Selected set of instructions from the IAS computer is given in Table Q2. Suppose that you are required to add the content from memory locations 0010 and 0011 and to store the result at the 0101.

i) Using the symbolic representation in Table Q2, list the set of the instruction to carry out the given operation.

[4 Marks]

ii) Using the symbolic representation in Table Q2, list the set of the instruction to store 54 to the memory location 0111.

[1 Mark]

Q3 a) i) State one advantage and disadvantage of SSD drives when compared to traditional magnetic drives.

[1 Mark]

ii) State why RAID drives are important in data storage.

[0.5 Marks]

b) i) Briefly explain the write-back and write-through techniques used in cache memory.

[2 Marks]

ii) Consider a processor consisting of one level of cache. Suppose that it exhibits a memory access time of 60 nanoseconds when cache miss ratio is 100%, and 10 nanoseconds when cache miss ratio is 0%. Evaluate average memory access time of this system when the cache hit ratio is 95%.

[2 Marks]

iii) Suppose that you are dealing with a main memory of 4 MB along with a cache memory of 64 kB. The cache memory consists of 16 byte cache blocks and it employs 4-way set associative mapping.

I. Calculate the number of cache lines.

II. Calculate the number of sets.

III. Calculate the tag length.

IV. Identify the set number corresponding to the memory address 0x349AC8.

Note: Consider mega as 2^{20}.

[5 marks]

c) i) Suppose that you are requested to identify a mechanism to detect errors of transmitted data packets at the receiver end. Calculate the number of additional bits that are required to identify single bit errors of 16-bit data packets using Hamming codes?

[1 Mark]

ii) Suppose that a data packet is encoded using a Hamming code. If the total length is 10 bits, evaluate the bit positions of the Hamming code (assume that the bit positions are from 1 to 10).

[1 Mark]

Q4 a) Suppose that you have to carry out the binary division of 3-bit binary numbers 111/010. Carryout the 2's complement division by using the format given in Figure Q4.

[4 Marks]

b) Briefly describe the following.

i) Reliability of symmetric multiprocessor systems

[1 Mark]

ii) Difference between a thread and a process

[1 Mark]

iii) Non-Uniform Memory Access (NUMA)

[1 Mark]

c) Suppose that a processor architecture supports a 5-stage pipeline.

i) Calculate the speedup of the pipeline for 100 instructions.

[1 Mark]

ii) Briefly explain what a resource hazard is.

[1 Mark]

iii) Suppose that out of the 100 instructions 10% are branch instructions while branch prediction is 90% accurate. Calculate the speedup of the pipeline, clearly stating your assumptions.

[3.5 Marks]

Table Q1

Instruction Type	Number of instructions	Duration per instruction (clock cycles)	Can parallelize?
Data Transfer	7	4	Yes
Arithmetic	8	5	Yes
Branch instructions	4	10	No
Address modify	2	9	Yes

Table Q2

Instruction Type	Opcode	Symbolic Representation	Description
Data Transfer	00001010	LOAD MQ	Transfer contents of register MQ to AC
	00001001	LOAD MQ, M(X)	Transfer contents of memory location X to MQ
	00100001	STOR M(X)	Transfer contents of AC to memory location X
	00000001	LOAD M(X)	Transfer M(X) to AC
Arithmetic	00000101	ADD M(X)	Add M(X) to AC; put the result in AC *M(X) can be an address name or a value
	00000110	SUB M(X)	Subtract M(X) from AC; put the result in AC
	00001100	DIV M(X)	Divide M(X) by AC; put the quotient in MQ and the remainder in AC

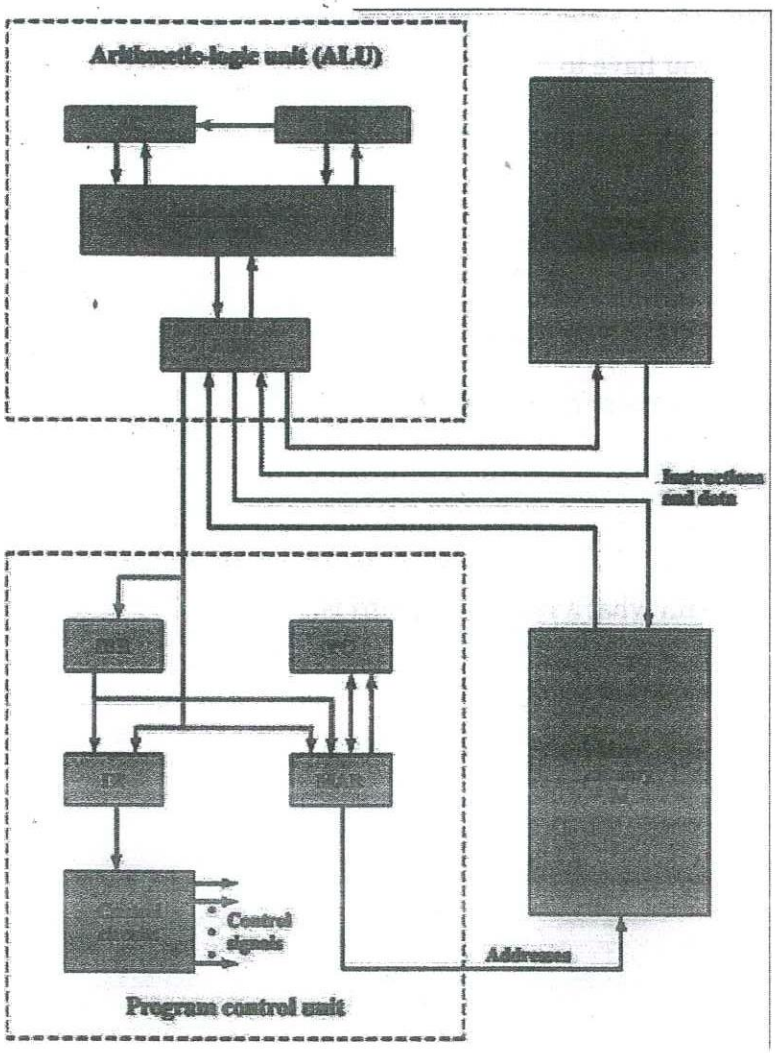

Figure Q2

	A			Q		

Figure Q4