UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 4 Examination in Engineering: December 2022

Module Number: ME4210 **Module Name: Analog and Digital Electronics**

[Three Hours]

[Answer **all questions**, each question carries **12** marks]

This paper contains **5 questions** on **6 pages**.
Clearly state any assumptions that you may make.
In order to get **full marks**, make sure to use standard notations and SI units, where appreporiate.

Q1. (a) Explain the operation of a relay using suitable circuit diagrams. List **two** applications of it.

[2.0 Marks]

(b) Figure Q1(b) shows a relay R_2 that is triggered by a square shape clock waveform Cp with a 5 V amplitude and 1 kHz frequency.

(i) What is the purpose of the diode D1 in the circuit.

(ii) Plot the Cp and the output waveform ($V_{out\,2}$).

[2.5 Marks]

(c) (i) Briefly describe two basic functions of a transistor.

(ii) Draw the output waveform (V_{out}) of the circuit given in Figure Q1(c) for a square shape clock waveform (Cp) with a 5 V amplitude and a 1kHz frequency.

(iii) Identify the circuit configuration in Figure Q1(c) and comment on its function.

[3.0 Marks]

(d) (i) Briefly describe the meaning of static hazard and dynamic hazard caused in combinational logic circuits.

(ii) Draw a timing diagram of the output G of the logic circuit shown in Figure Q1(d) for the given input signals by taking the propergation delay into account.

(iii) State any issue in the output of the circuit and draw an improved version of circuit avoiding the issue.

[4.5 Marks]

Q2. (a) D, JK, and T are the three types of flip-flops that can be used to make sequential circuits.

(i) Draw a D type flip-flop with correctly marked pins and write down its characteristic equation.

(ii) Draw the JK type flip-flop with correctly marked pins and write down its characteristic equation.

(iii) Draw the T type flip-flop with correctly marked pins and write down its characteristic equation.

[3.0 Marks]

(b) A sequential circuit is to be designed as a component of the power management system of a house, which has grid connected power combined with a solar panel system and a battery backup system. The system should operate as given below.

Inputs to the system:

x1 - high when grid power is precent
x2 - high when solar panels can fulfill the power demand
x3 - high when the batteries have reached the fully charged limit
x4 - high when the batteries have reached the fully discharged limit

The states of the flip-flops are taken as binary assignments and control these connections.

1. House is connected to the grid power
2. House is connected to solar panels
3. House is connected to batteries

Solar panels will charge the batteries at all times.

1. House will be connected to the grid power when the grid power is present.
2. If *x2* is high, house will be connect to the solar panels from grid and if *x2* is low, House will be connected to the grid power. As long as x2 is high even if the grid power is lost, the house will remain connected to the solar panels.
3. When there is no power on the grid, house will be connected to batteries. House will be connected to batteries as long as there is no power on the grid and even batteries are dead, and solar panels can supply the demand.
4. When the power is back, the house will be re-connected to the grid
5. The house cannot connect directly from solar panel to battery and vise versa. It has to go through the grid connection.

Based on the above case, answer the following questions.

(i) Construct the state diagram for the given system.

(ii) Breifly explain whether the state reduction is possible. If so, do the state reduction.

(iii) Assign the states using binary numbers.

(iv) Construct the state table using D-type flip-flops.

(v) Construct the sequential circuit.

[9.0 Marks]

Q3. (a) Using the Karnaugh map method, simplify each of the following logic functions:

(i) $E(A,B,C,D) = \sum m(0,2,4,5,10,12,15)$

(ii) $F(A,B,C,D) = \sum m(0,2,4,5,10,12,15) + \sum x(18,14)$

[3.5 Marks]

(b) You are asked to design a circuit to switch in four directions packages identified by an eight-bit binarycode $I_7I_6I_5I_4I_3I_2I_1I_0$ where I_7 is the most significant bit. The signal D_0 is set at 1 if no direction is chosen. Based on the code of each packet, the switchching is carried out as follows.

$D_1 = 1, if\ 32 \leq N \leq 63$
$D_2 = 1, if\ 64 \leq N \leq 127$
$D_3 = 1, if\ 128 \leq N \leq 159$
$D_4 = 1, if\ 192 \leq N \leq 255$

The number N being the decimal number corresponding to the binary-code $I_7\ I_6\ I_5\ I_4\ I_3\ I_2\ I_1\ I_0$.

(i) Determine the Boolean expression for the logic function for the selection of each of the directions ($D_0, D_1, D_2, D_3,$ and D_4).

(ii) Draw the circuit required to implement above functions using only logic inverters and NAND gates with at most three inputs ($I_7I_6I_5$).

[8.5 Marks]

Q4 (a) Describe a function of a digital filter and what steps to be performed to bring a raw analog signal to a filtered analog signal using suitable block diagrams and wave forms.

[2.0 Marks]

(b) For each of the following filters, state the order of the filter and determine the values of its coefficients.

(i) $y_n = 2x_n - 2x_{n-4} + x_{n-2} - 3x_{n-1}$

(ii) $y_n = 2x_n - y_{n-2} + y_{n-1} + 5x_{n-1}$

[2.0 Marks]

(c) Breifly describe five parameters of a practical filter. Plot the magnitude of a suitable filter transfer function ($|H(\omega)|$) vs frequency (ω) and indicate all the five parameters.

[5.0 Marks]

(d) A low-pass Butterworth filter is to be designed to meet the following design criteria:

Passband
Nominal gain, $A_{V0} = 1$
Passband edge, $f_C = 4\ kHz$, $\gamma_{max} = 1.2\ dB$ maximum

Q4 is continued to page 4

Q4 is continued from page 3

Stopband
$f_S = 15\ kHz, \gamma_{max} = 40\ dB$ minimum.
Determine the Butterworth design partameters (the order and the resonant frequency in Hz).

Given that,
The Butterworth polynomial (a third order degree of freedom):

$$|B_n(\omega)| = \sqrt{1 + \varepsilon^2 \left(\frac{\omega}{\omega_C}\right)^{2n}}$$

The resonant frequency of the filter:

$$\omega_0 = \frac{\omega_C}{\sqrt[n]{\varepsilon}}$$

[3.0 Marks]

Q5. (a) Briefly explain why Programmable Logic Controllers (PLCs) are preferred over microcontrollers when it comes to industrial applications.

[2.0 Marks]

(b) Briefly describe the main steps of the operating cycle of a PLC.

[2.0 Marks]

(c) List **four** advantages of PLCs compared to conventional relay control systems.

[2.0 Marks]

(d) To maintain uniform product quality, an automated painting process has been purposed to be implemented at an automobile spare parts production facility. There, following the machining process, the parts are transported to the painting section via a conveyer line and, to get two coats of paint before proceeding to the next process. The layout of the process is given in Figure Q4(d), and it is supposed to perform the following functions:

- When the presence of a part is identified by "Sensor 1", the conveyer stops for 5 s and activates the "Spray Nozzle 1" for 3 s to apply the first paint coat.
- When the presence of a part is identified by the "Sensor 2", the conveyer stops for 4 s and activates the "Spray Nozzle 2" for 2 s to apply the second paint coat.
- Two liquid level sensors (LLS 1 and LLS 2) are used to continuously monitor the paint level in the paint tanks, and if the levels get lower than a pre-set value, an "Alarm" will get activated to alert the supervisor and the conveyer will remain stopped until the liquid level becomes back to normal.
- A "Zero Speed Sensor" is used to monitor the status of the conveyer. If the conveyor stops for any reason, the "Alarm" will get activated.

Q5 is continued to page 5

Q5 is continued from page 4

- The fully automated system is to be activated using a master switch.

Draw the input/output mapping table and develop a ladder logic program for the above application.

[6.0 Marks]

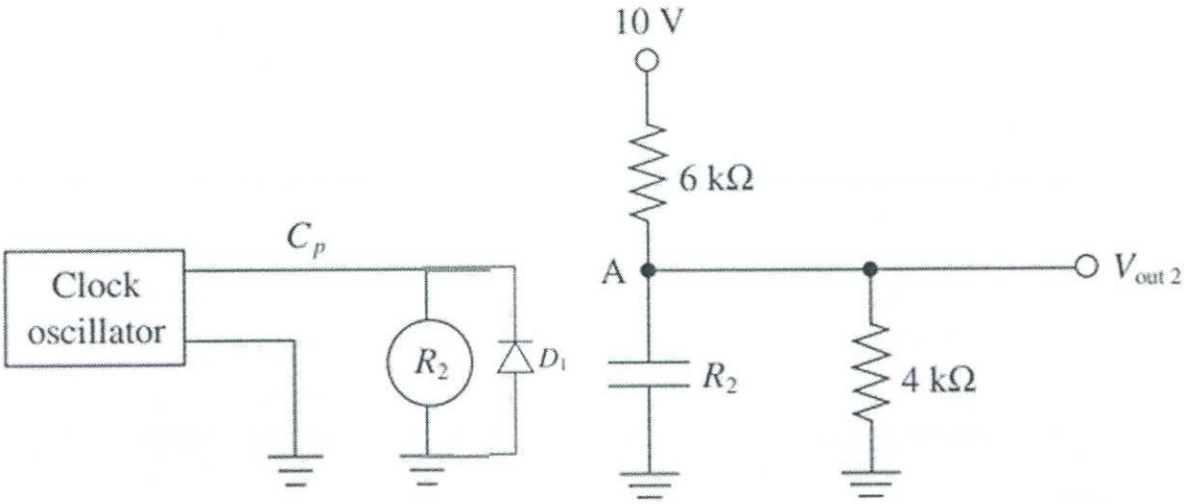

Figure Q1(b)

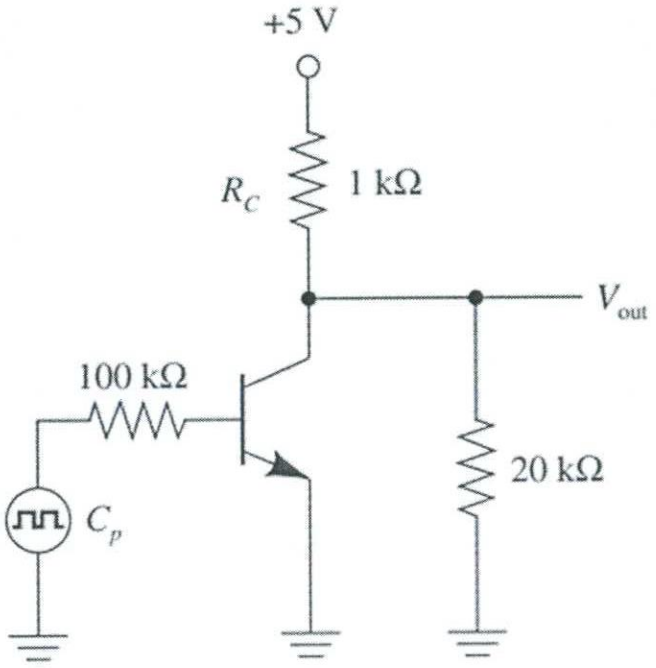

Figure Q1(c)

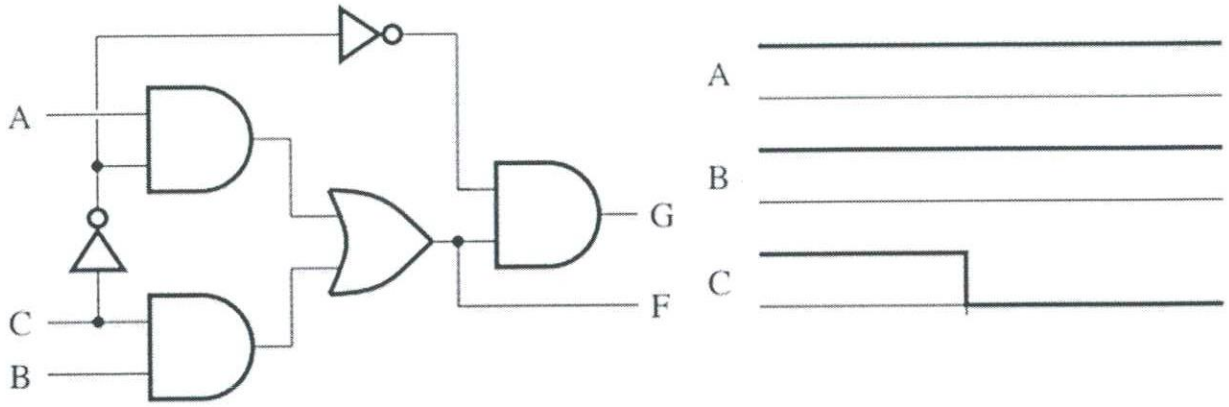

Figure Q1(d)

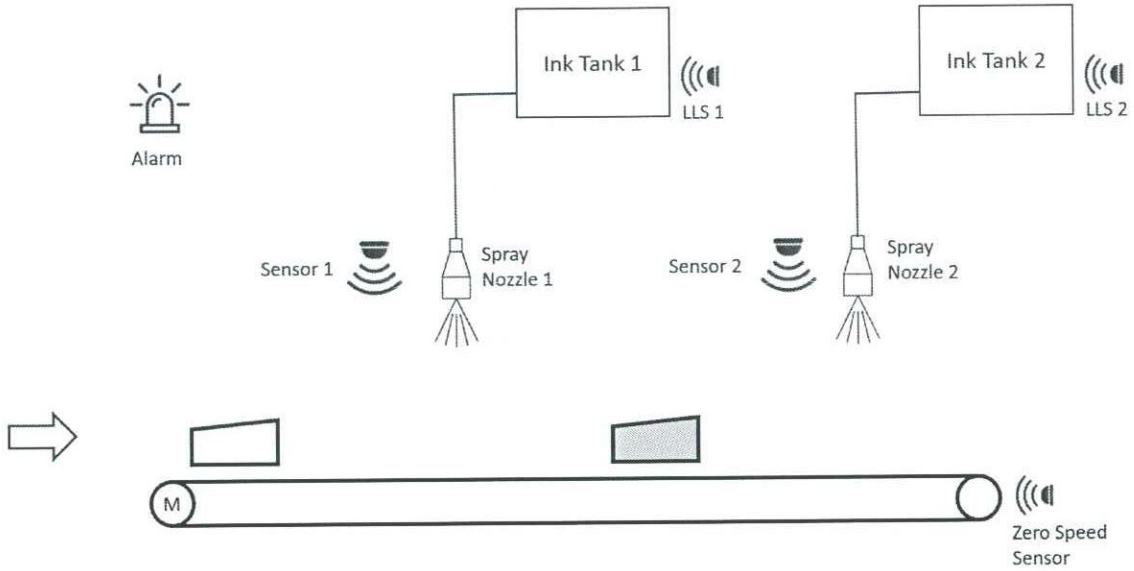

Figure Q5(d) - Layout of the automated painting process