University of Ruhuna - Faculty of Technology

Bachelor of Information & Communication Technology
Level 1 (Semester 2) Examination – April 2019

Department: Information & Communication Technology

Course Unit: ICT1252 (Computer Architecture)-Theory **Time: 2 hours**

Answer all **four (4)** questions

---

1)

a)

i) Write down **two (2)** methods to handle multiple interrupts

ii) The following **Figure 1** shows an instruction cycle with interrupt handling. Name components of the **Figure 1** marked from A to G.

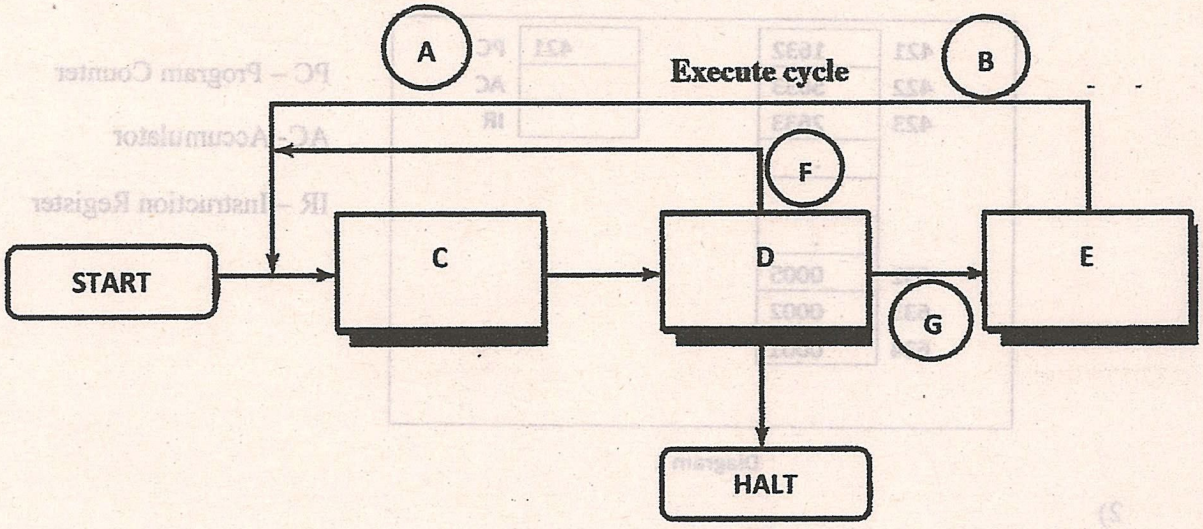


Figure 1

b)

i) Write down **four(4)** main functions of a computer.

ii) Briefly explain the purpose of **Memory Address Register** and **Memory Buffer Register** separately.

iii) Name the **four(4)** main structural components of the Central Processing Unit and write down the main functionality of each of them.

c.

ii. Briefly explain the difference between dedicated and multiplexed buses.

iii. The following **Diagram 1** shows the states of memory and CPU registers before executing an instruction. Draw the steps of adding content of memory location 632 to the content of memory location 633. Explain each step briefly.

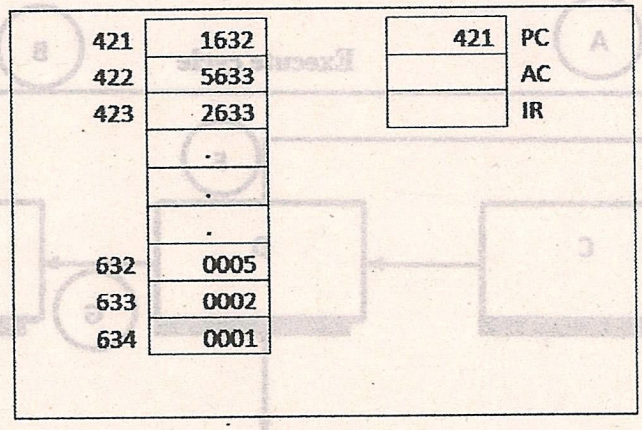
(**Note**: Consider that both instructions and data are 16 bits long)

Use the following list of op codes.

0001 – Load AC from memory

0010 – Store AC to memory

0101 – Add to AC from memory)



PC – Program Counter

AC- Accumulator

IR – Instruction Register

Diagram 1

2)

a)

i) Replacement algorithms are used in the associative and set-associative cache memory mappings. Name the algorithms used for the following purposes.

(1) To replace the block in the set that has been in the cache for longest time without referencing.

(2) To replace the block, which has experienced the fewest number of references.

(3) To replace the block in the set that has been in the cache for longest time.

ii) Briefly explain how read operation happens in the cache, when the CPU requests content of a memory location.

iii) Cache addressing can be categorized into two types by considering the location where the cache is situated. Name those **two (2)** cache addressing types and write down how cache is located in those two cache addressing types.

b)

i) The substrate of a magnetic disk is made by glass recently. Write **two (2)** advantages of using glass instead of aluminum as the substrate.

ii) Explain the read (traditional) and write mechanisms of a magnetic disk.

c)

i) Explain the direct, associative and set-associative memory mapping techniques briefly.

ii) Consider a memory system that uses 64 bit long addresses to address at the byte level, and a cache with a 128 byte cache line size. Assume a **two-way set associative** cache with a 12 bit long tag field in the address.

Calculate the values of following paramaters

(1) Number of addressable units in the main memory.

(2) Number of bits in a word.

(3) Number of blocks in the main memory.

(4) Number of sets in cache

(5) Number of lines in cache memory.

(6) Draw the address structure with the values and name all the sections of the address.

3)

a)

i) Briefly explain the meaning of **pipeline hazards.**

ii) Name **three (3)** types of data hazards

iii) Explain the meaning of **instruction prefetch** briefly.

b)

i) Write down the steps followed in accessing a random address in a CD-ROM.

ii) Fill in the blanks of the following **Table 1** which shows the characteristics of internal memory types.

Memory Type	**Erasing mechanism**	**Write Mechanism**	**Volatility**
Flash Memory	Electrically	Electrically	Non-volatile
Random Access Memory (RAM)	.....	.....	.....
Erasable Programmable ROM (EPROM)	.....	.....	.....
Electrically Erasable PROM (EEPROM)	.....	.....	.....

Table 1

c)

i) Fill in the blanks in **Table 2** and calculate the check bits for the data word 1101 using hamming error correction code. Write down the bit position, position number, data bits and check bits for the given data word.

Bit position							
Position number							
Data bits							
Control bits							

Table 2

ii) Consider that there is an error with the least significant bit of the data word given in 3)c)i). Assume the new word is 1100.

(1) Calculate the new check bits.

(2) Calculate the syndrome word and prove that the least significant bit has the error.

4)

a)

i) List **four (4)** elements of a machine instruction.

ii) Apply each of the following operation three times on the data word, 11011100 and write down the answers separately

1. Logical left shift
2. Arithmetic right shift
3. Arithmetic left shift
4. Right rotate

b)

i) Name the **three (3)** most common displacement algorithm types.

ii) Using a diagram, represent the displacement addressing mode and name all the components.

c)

i) Using 4-bit two's complement notation, solve the mathematical calculation (-4)+(-3). Explain whether in any register, overflow exist or not in this operation.

ii) Given below is a floating point number in 32 bit representation. Calculate the true exponent value in decimal. Show all the intermediate steps.

1 10010101 10100010000000000000000

iii) Multiply -4 (multiplicand) by 6(multiplier) using Booth's Algorithm. Use 4-bit binary representation and clearly write down all the intermediate steps you follow.

iv) Convert the answer you obtained in 4) b) iii) in to decimal. Clearly write down the steps you follow.

********** End **********