UNIVERSITY OF RUHUNA

Faculty of Engineering

Mid-Semester 3 Examination in Engineering: June 2014

Module Number: EE3306 **Module Name: Analog Electronics**

[Two Hours]

[Answer **all questions**, each question carries 5 marks each]

Q1

a) Explain briefly the functions of the following fundamental components of a DC power supply.

i) Rectifier

ii) Low-pass filter

iii) Voltage regulator

[1 Mark]

b) Draw the circuit diagram of a full-wave bridge rectifier with a capacitor filter and the waveform that results when a sine wave is input.

[1 Mark]

c) i) By clearly stating your assumptions, show that the percent ripple in the output of a rectifier with a capacitor filter can be given as,

$$r = \frac{1}{2\sqrt{3} f_r R_L C} \times 100\%$$

(All the notations have their usual meanings)

ii) A full wave rectifier is operated from a 120 V rms, 50 Hz line and has a capacitor filter connected across its output. What minimum value of capacitance required if the load is 200 Ω and the ripple must be no greater than 4%?

iii) Calculate the average current in the load.

[3 Marks]

Q2 a) Explain briefly the purpose of voltage regulation in a DC power supply with an ac source. [1 Mark]

b) A DC power supply with a Zener diode voltage regulator shown in Figure Q2 (b) supplies power to an application where the Zener diode is used as a highly stable voltage reference. Show that the resistance R_s should lie within the following limits to achieve proper voltage regulation.

$$\frac{V_{in(max)} - V_Z}{I_{z(max)} + I_{L(min)}} \leq R_s \leq \frac{V_{in(min)} - V_Z}{I_{z(min)} + I_{L(max)}}$$

(All the notations have their usual meanings) [1.5 Marks]

c) You are given three resisters of 400Ω, 500Ω and 1kΩ to design the regulator circuit in part b). Select appropriate resistor(s) for R_s according to the following requirements.

- $3mA \leq I_z \leq 300mA$
- The input voltage waveform to the regulator circuit is in the form given in Figure Q2 (c).
- The load is a variable resistor of 50kΩ to 100kΩ

[2.5 Marks]

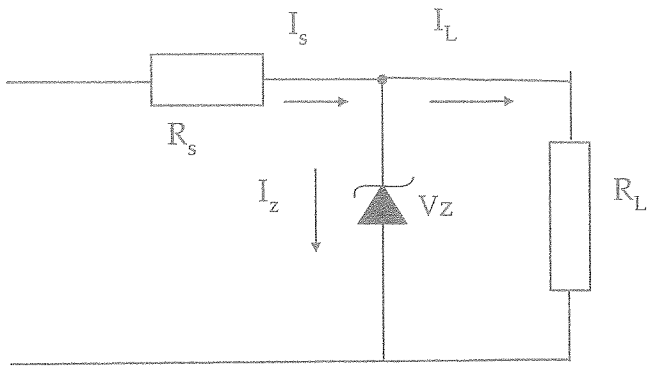

Figure Q2 (b)

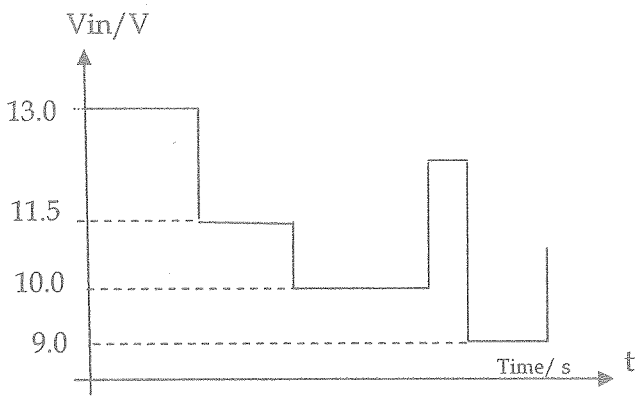

Figure Q2 (c)

Q3 a) Fig Q1 shows an amplifier circuit based on a Si transistor having $\beta = 60$ connected to a source $v_s = 10 \text{ Sin } 10^3 t$

i) Calculate the voltage gain A_v for the amplifier.

ii) Calculate the input and output resistances, r_{in} (s) and r_o(s) respectively of the amplifier stage.

iii) Determine a value for the capacitor C.

iv) If a load voltage RL = 50 Ω is connected at the output, what is the overall voltage across the load and the overall voltage gain of the circuit?

v) Why is the overall voltage gain much less than the amplifier voltage gain.

[2.5 Marks]

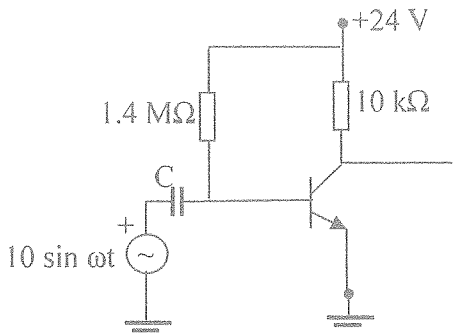

Figure Q3

b) i) What factors affect the parameter values of transistors?

ii) How do the values of β and collector-to-base leakage current I_{CBO} affect the Q point of an amplifier?

iii) How can the amplifier circuit in Figure Q1 be modified to minimize the effects of parameter variability?

iv) What is the amplifier voltage gain for the modified circuit?

v) How can the change in the voltage gain be minimized?

[2.5 Marks]

Q4 a) Define the current and voltages for a 2 port network. [0.5 Marks]

b) Define the h parameters for this 2 port network [1 Mark]

c) What is the hybrid equivalent circuit that can be substituted for any network where the h parameters are known?? [1 Mark]

d) Draw the h parameter equivalent circuit for a Common-Emitter amplifier with a source of voltage v_s with source impedance r_s and load impedance Z_L. [1 Mark]

e) Derive expressions for the overall voltage and current gains for the h parameter equivalent circuit in d). [1.5 Marks]