UNIVERSITY OF RUHUNA – FACULTY OF TECHNOLOGY

BACHELOR OF ENGINEERING TECHNOLOGY

Level II (Semester II) Examination, April 2019.

Course Unit: ENT2213 Digital Electronic Systems

Time Allowed Three Hours

[Answer **All (4) Questions**]

Instructions

- This question paper consists of 4 questions. All questions must be answered.
- All answers to new questions should start in a new page, and all the answers to each question should be organized together.
- All calculations should be shown, and all assumptions stated clearly.
- This is a closed book exam and therefore no study material is allowed during the exam.
- Calculators and cell phones are strictly prohibited.

01.

a) Write down the 8-bit binary representation of 47, show your work clearly.
b) Write down 2's compliment, 8-bit representation of -93, show your work clearly.
c) Do the following arithmetic operations using the 8 bit binary representation of the numbers, show your work clearly.
   I. 14×3
   II. $24 \div 8$
d) Add the following 8 bit 2's compliment binary numbers and indicate which ones have an overflow error. Show your work clearly and why and how you decided there is an overflow error.
   I. 00011010 + 11000001
   II. 10001001 + 11010001
   III. 01100001 + 11010001
e) Draw gate diagram and write the truth table of the following gates NOT, OR, AND, NOR, and NAND gates. (Not gate is done for you)

NOT		OR			AND			NOR			NAND		
													
A	Q	A	B	Q	A	B	Q	A	B	Q	A	B	Q
1	0	0	0		0	0		0	0		0	0	
0	1	0	1		0	1		0	1		0	1	
X	X	1	0		1	0		1	0		1	0	
X	X	1	1		1	1		1	1		1	1	

f) NAND gate is one of the universal gates used in digital electronics, Show the construction of NOT, AND, and OR gates using NAND gates. (hint- a NAND gate is a negative OR gate)

02.

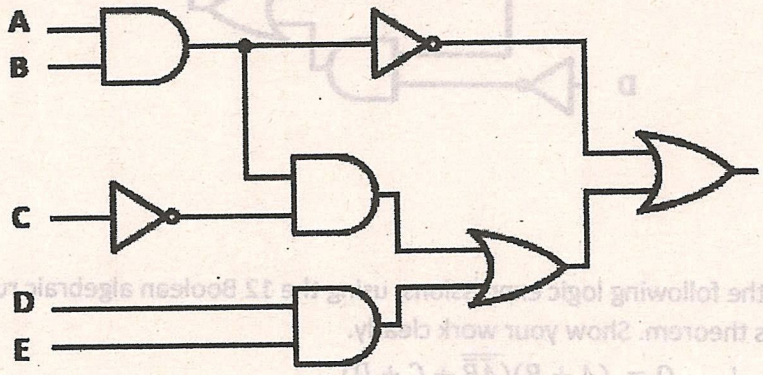
a) Write the SOP (Sum of Products) and the POS (Product of Sums) expressions for the following truth table, where A, B, C and D are inputs and Q is the output.

A	B	C	D	Q
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

b) Draw the Karnaugh map for the above truth table and find the minimized SOP and POS expressions using the Karnaugh map, show all the groups clearly and the terms corresponding to the each of the groups. Use two separate Karnaugh maps for SOP and POS groups.

c) Draw the combinational logic diagram for the above truth table (minimized) **SOP (Sum of products)** using only the AND, OR, and NOT gates

d) Draw the equivalent NAND only logic implementation for the combinational logic circuit below.



e) Draw the Karnaugh map for the following scenario,

A room is equipped with four, A, B, C, and D, sensors as below.

A – An IR motion sensor that gives 1 (High) if the room is occupied (if anyone is present in the room), and 0 (Low) if the room is empty.

B – A light switch sensor that gives 1 (High) if any of the light switches are turned ON, and 0 (Low) if all the switches of off

C – An air conditioner switch sensor that gives 1 (High) if the air conditioner switche is turned ON, and 0 (Low) if the switch is off

D – A voltage sensor that gives 1 (High) if the main power supply is OK, and 0 (Low) if there is a power loss in from the main grid.

The building has an automatic switch that turns ON (state 1/High) a generator if all of the below conditions are true,

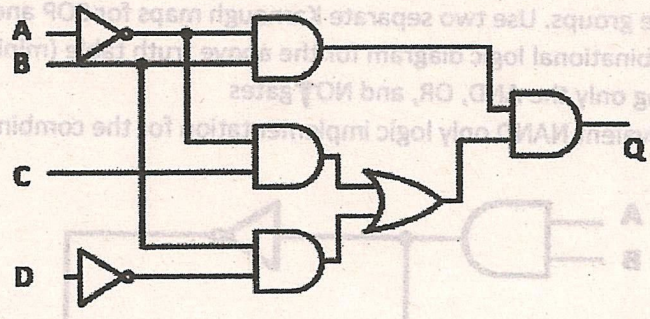
1. The room is occupied (someone present) in the room and
2. At least one of the electric equipment (lights/ Air conditioner) is ON
3. The power from the main power supply is lost

or else will stay OFF (state 0/Low).

f) Find the **minimized SOP (Sum of products)** expression for the generator switch

03.

a) Write down the output expression for the following circuit



b) Simplify the following logic expressions, using the 12 Boolean algebraic rules and the De-Morgan's theorem. Show your work clearly.

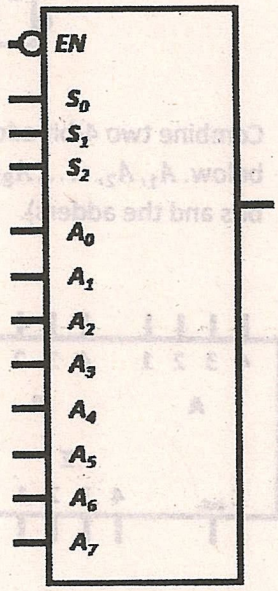
I. $Q = (A + B)(\overline{\bar{A}\bar{B}} + C + D)$

II. $Q = [A\bar{B}(C + BD) + \bar{A}\bar{B} + \bar{D}]C$

$$A + 0 = A \qquad A \cdot A = A$$
$$A + 1 = 1 \qquad A \cdot \bar{A} = 0$$
$$A \cdot 0 = 0 \qquad \bar{\bar{A}} = A$$
$$A \cdot 1 = A \qquad A + AB = A$$
$$A + A = A \qquad A + \bar{A}B = A + B$$
$$A + \bar{A} = 1 \qquad (A + B)(A + C) = A + BC$$
$$\overline{AB} = \bar{A} + \bar{B} \qquad \overline{A + B} = \bar{A}\bar{B}$$

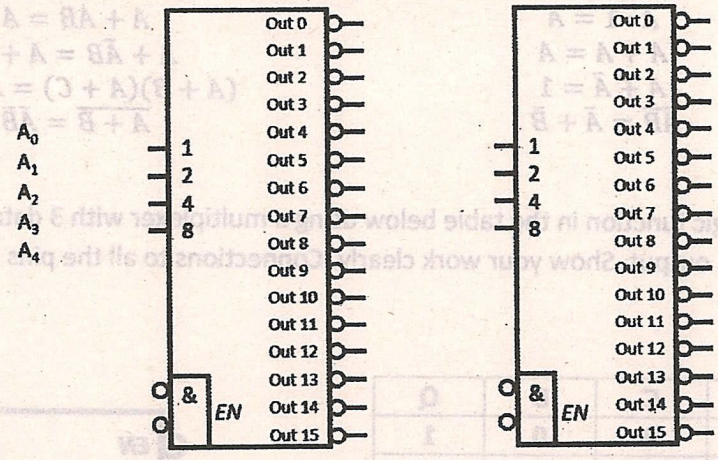
c) Implement the logic function in the table below using a multiplexer with 3 data select inputs, 8 data inputs, and 1 output. Show your work clearly. Connections to all the pins should be shown clearly.

A	B	C	D	Q
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

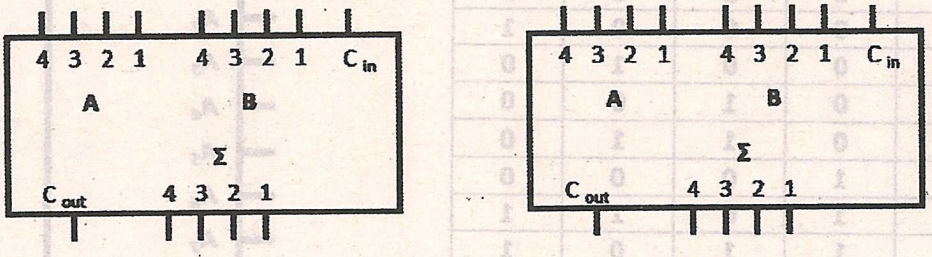


d) Connect the following components to achieve the following tasks (Pay attention to the active low and active high inputs/outputs)

I. Combine two *4-line-to-16-line* decoders to achieve a 5-line-to-32-line decoder. In your diagram indicate the 0 to 31 output pins clearly



II. Combine two 4-bit adders to achieve a 8-bit adder, use two 4 bit adders as shown below. $A_1, A_2, \ldots\ldots, A_8, and\ B_1, B_2, \ldots\ldots, B_8$. Clearly show the wiring between each of the bits and the adders).



04.

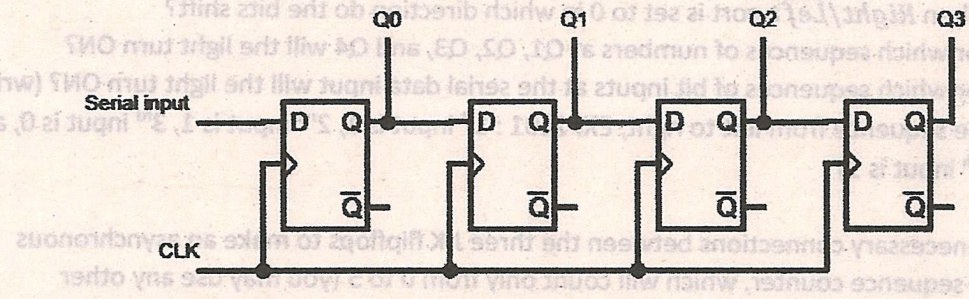
a) Complete the following tables for the given Latches and Flip-Flops, active low input (a) $\bar{S} - \bar{R}$ latch, (b) D Flip-Flop, and (c) J-K Flip-Flop.

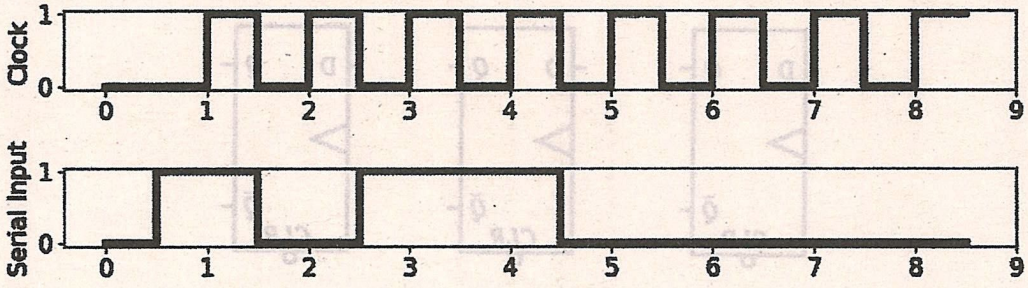
(i) J-K Flip Flop				
Input			Output	
J	K	CLK	Q	$\bar{Q}$
0	0	↑		
0	1	↑		
1	0	↑		
1	1	↑		

(ii) D Flip Flop			
Input		Output	
D	CLK	Q	$\bar{Q}$
0	↑		
1	↑		

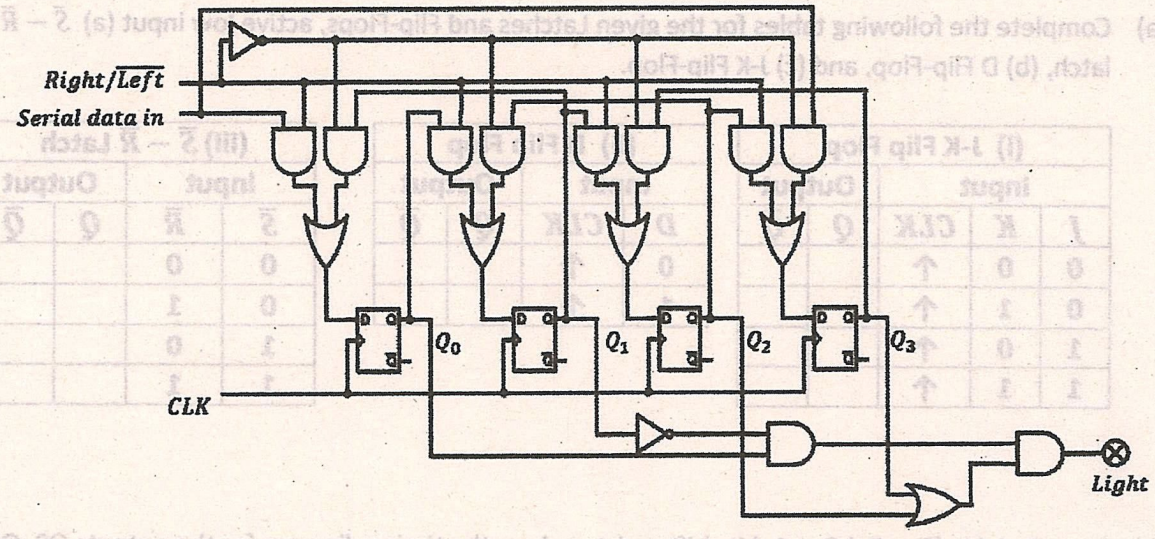
(iii) $\bar{S} - \bar{R}$ Latch			
Input		Output	
$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$
0	0		
0	1		
1	0		
1	1		

b) For a Serial In/Parallel Out 4 -bit shift register, draw the timing diagram for the outputs Q0, Q1, Q2 and Q3 for the given input below (10110000). Initial state



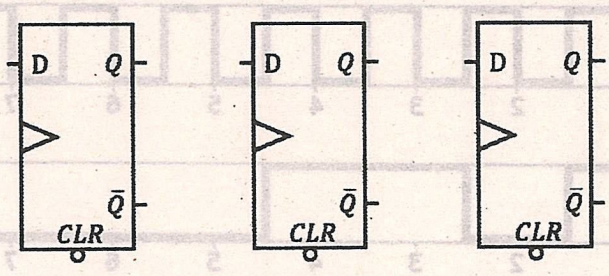


c) Shown below is a combinational circuit connected to a bidirectional D flip-flop shift register.

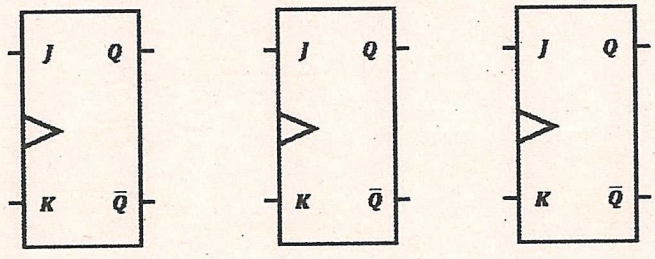


I. When $Right/\overline{Left}$ port is set to 0 in which direction do the bits shift?
II. For which sequences of numbers at Q1, Q2, Q3, and Q4 will the light turn ON?
III. For which sequences of bit inputs at the serial data input will the light turn ON? (write the sequence from left to right, EX: 1101 : 1st input is 1, 2nd input is 1, 3rd input is 0, and 4th input is 1)

d) Make the necessary connections between the three J-K flipflops to make an asynchronous truncated sequence counter, which will count only from 0 to 5 (you may use any other necessary gates).



e) Write down the three bit binary sequences for an up count (0 to 7) and a down count (7 to 0). Using these sequences and considering the times at which the flip flops toggle, build an up/down synchronous counter using three J-K flip-flops. The counter should have the ability to count both up and down, and the choice is made with a single input $UP/\overline{DOWN}$ (you may use any other logic gates necessary).



f) Calculate the output voltage of the following DAC circuit if the input is 1010.