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University of Ruhuna - Faculty of Technology

Bachelor of Engineering Technology Honours Degree
Level 2 (Semester I) Examination, July 2023
Academic year 2021/2022

Course Unit: ENT 2113 – Analogue Electronic Systems (Written)

Duration: 3 hours

- This paper contains **five (05)** questions on **four (04)** pages.
- Answer all the questions.
- This is a **closed book** examination.

Q1.

A rectangular intrinsic Si semiconductor plate having the dimensions of 0.6 cm length and 2 $cm \times 2\ cm$ cross section is applied with a voltage of 12 V through the square shaped cross section.

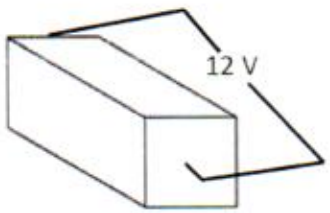

Figure 1a

Let the intrinsic carrier density $n_i = 1.5 \times 10^{10} electron/cm^3$,

the mobility of electrons $\mu_e = 0.14\ m^2V^{-1}s^{-1}$

and the mobility of holes $\mu_h = 0.05\ m^2V^{-1}s^{-1}$.

Take the charge of an electron as $e = 1.6 \times 10^{-19}$ C.

a) Find the **drift velocities** of electrons and holes. (02 marks)
b) What are the **current densities** created by the electrons and holes? (02 marks)
c) What will be the **total current density**? (01 marks)
d) Calculate the total current through plate considering the total current density calculated in part c). (01 marks)
e) Find the **conductivity and resistivity** of the intrinsic Si on the plate. (02 marks)
f) Find the current through the plate considering the voltage and resistance. (02 marks)

Q2.

A sinusoidal voltage of peak value **15 *V*** is fed through a Si diode of knee voltage **0.7 *V***.to a load of **10 *kΩ***.

a) Sketch the shape of the output voltage through the load and indicate its peak value. (02 marks)

b) What is the **peak current** corresponding to the positive half-cycle of the input signal? (01 marks)

c) Find the **maximum reverse voltage** through the diode corresponding to the negative half cycle of the input signal. (02 marks)

d) What happens when this maximum reverse voltage is higher than the peak inverse voltage of the diode? (01 marks)

Assume the diode in the setup was replaced with an ideal diode and was connected to the secondary side of a step-down transformer whose turns ratio is 8: 1. If the primary was connected to the domestic supply,

e) What is the **peak value** of the voltage through the load? (02 marks)

f) What is the **DC current** through the load? (02 marks)

Q3.

a) Obtain expressions for the **voltage gain** A_v and the **current gain** A_i of a transistor circuit in the **common collector configuration**. Hence show that the power gain is given by, $A_p = 1 + \beta$. (03 marks)

Figure 3*a* shows an ***npn* Si transistor** in the **common emitter configuration** whose DC voltage gain $\beta_{DC} = 200$, biased using the voltage divider method, with an input voltage signal (v_s) of peak is 1 mV. The AC voltage gain of the transistor is 150.

$R_{B1} = 24\ k\Omega, R_{B2} = 12\ k\Omega, R_L = 4\ k\Omega, R_E = 5\ k\Omega$ and $V_{CC} = 24\ V$.

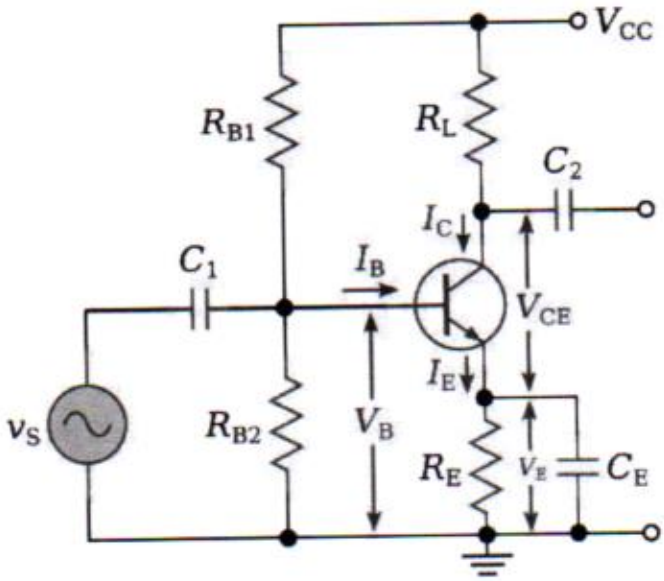

Figure 3a

b) What is the reason for the use of each capacitor in the circuit? (02 marks)
c) Give **two (02)** advantages of using an **emitter resistor**. (02 marks)
d) Indicating the necessary values, sketch how the input and output voltages of the transistor fluctuate with time. (05 marks)

Consider the same Figure 4*a* without the input voltage and the capacitors.

e) Obtain the equation of the DC load line. (02 marks)
f) Hence draw the load line for this circuit. (03 marks)
g) Find the Q point and show that it satisfies the equation of the DC load line. (03 marks)

Q4.

a) Show that the circuit in Figure 4a depicts a **logarithmic amplifier**.
(Hint: $i_d \approx I_0 e^{-v_D/v_T}$) (03 marks)

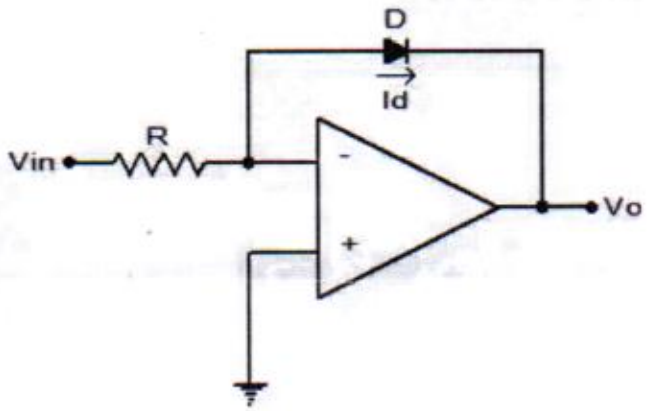

Figure 4a

b)

i. Obtain the relationship between the input and the output voltages of the circuit shown in Figure 4b. (03 marks)
ii. Hence find the **mathematical operation** this circuit. (01 marks)

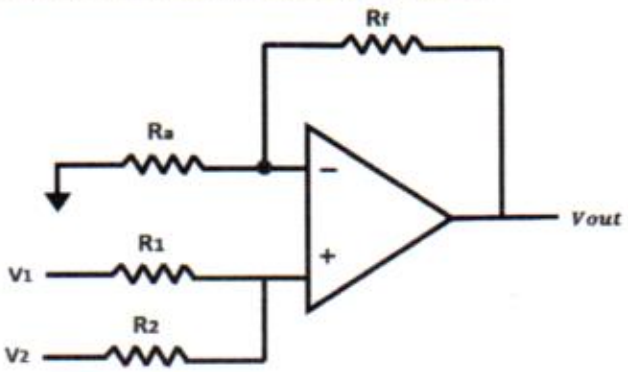

Figure 4b

c) Consider an inverting amplifier having two resistors R_1 and R_f at the input and feedback, respectively. **Show that** when the open loop gain approaches infinity, the voltage difference $(V_-) - (V_+)$ of the Op Amp approaches zero. (03 marks)

Q5.

Modulation refers to modifying a carrier signal, which is a high-frequency waveform, by adding information from a lower-frequency signal called the modulating signal.

a) Calculate the **size of the antenna** to receive a message signal of frequency $4\ kHz$ transmitted through free space without modulation. (02 marks)

b) A message signal $\boldsymbol{m(t) = A_m \cos 2\pi f_m t}$ is mixed with a carrier signal $\boldsymbol{c(t) = A_c \cos 2\pi f_c t}$ in a double sideband suppressed carrier (DSB SC) modulation scheme. By carrying on the necessary calculations, sketch the **frequency spectrum** of the modulated signal $M(t)$ **in the complex domain**. (03 marks)

c) Assuming the signal received at the Receiver antenna $\boldsymbol{r(t) = A_c m(t) \cos 2\pi f_c t}$, and the output of the local oscillator $\boldsymbol{c'(t) = A_c \cos(2\pi f_c t + \phi)}$, show through necessary calculations, how the message signal $m(t)$ is **extracted** using DSB SC demodulation. (03 marks)

d) Mention **two (02) analogue electronic instruments** which are used in the modulation and demodulation processes. (02 marks)

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