UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 6 Examination in Engineering: November 2022

Module Number: EE6205 **Module Name: Hardware Description Language**

[Three Hours]

[Answer **all questions**, each question carries **10 marks**]

Q1 a) (i) Describe four (04) advantages of using HDL for electronic design over schematic diagrams.

[2.0 Marks]

(ii) Differentiate programming language for CPUs and Hardware Description Language.

[1.0 Mark]

b) (i) State two (02) main paths in VLSI design.

[1.0 Mark]

(ii) Compare ASIC and FPGA in terms of their pros and cons.

[2.0 Marks]

(iii) Explain the role of Test Bench in VLSI design verification.

[1.0 Mark]

c) As an electronic design engineer, you are asked to design a 4-way traffic light controller.

(i) Suggest three (03) design approaches to design the circuit.

[1.0 Mark]

(ii) Justify the use of HDL to design the above-mentioned system.

[2.0 Marks]

Q2 a) Name and describe two (02) main components of a VHDL design.

[1.0 Mark]

b) Why is it a good approach to draw a black-box diagram when using VHDL to model digital circuits?

[1.0 Mark]

c) Write the VHDL entity declaration that describes the black-box diagram shown in Figure Q2 c).

[3.0 Marks]

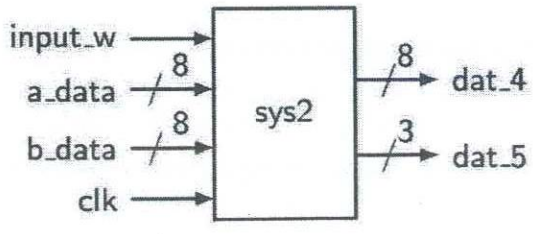

Figure Q2 c)

d) Name and explain the three (03) main modeling styles that can be used to describe the internal implementation of the associated entity.

[3.0 Marks]

e) Write a VHDL code to implement the following Boolean function using concurrent signal assignment.

$$F(A,B) = \bar{A}B + A + A\bar{B}$$

[2.0 Marks]

Q3 a) Explain the difference between types 'wire' and 'reg' in Verilog.

[1.0 Mark]

b) (i) Write a Verilog module to implement a 1-bit full adder and name it as **full_adder**.

[2.0 marks]

(ii) Design a 4-bit full adder using Verilog incorporating the **full_adder** module in Q3 b (i).

[3.0 marks]

(iii) Write two (02) Test Benches to test the 1-bit full adder and 4-bit full adder.

[4.0 Marks]

Q4 Figure Q4 shows a Serial-in Serial-out (SISO) Shift register.

a) Implement the SISO Shift register shown in Figure Q4 using VHDL.

[4.0 Marks]

b) Explain the difference between blocking and non-blocking statements in Verilog.

[2.0 Marks]

c) Implement the SISO Shift register shown in Figure Q4 using Verilog.

[4.0 Marks]

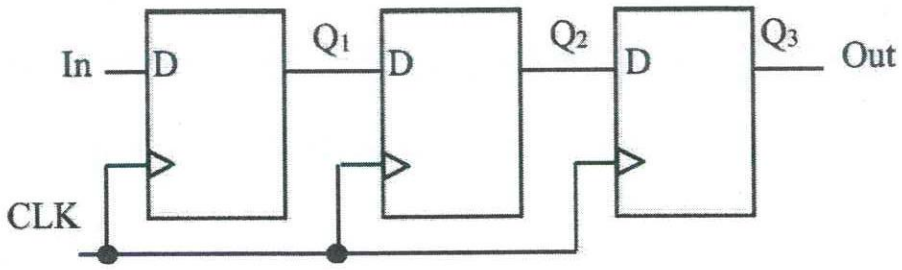

Figure Q4

Q5 a) Explain the role of LUTs and D Flip-flops in FPGAs.

[2.0 Mark]

b) State two (02) main constraint files required in FPGA.

[1.0 Mark]

c) Name and explain the standard way to communicate between 2 different modules in FPGA?

[1.0 Mark]

d) State two (02) main timing failures that happen in FPGA designs and explain how those timing failures are corrected.

[3.0 Marks]

e) Explain main steps of designing a digital system using FPGA.

[3.0 Marks]