University of Ruhuna- Faculty of Technology

Bachelor of Information and Communication Technology Honors Degree

Level I (Semester II) Examination, November/December 2023

Academic year 2021/2022

Course Unit: ICT1242 Computer Architecture (Written) Duration 2 ½ hours

IMPORTANT INSTRUCTIONS:

1. The medium of this examination is English.
2. This is a closed book examination.
3. This question paper contains **four (04) pages** including this instruction page.
4. This examination consists of **four (04) questions** that are given equal marks.
5. All symbols have their usual meanings.
6. Answer all the questions.

1.

a)

i. Define the terms ***"computer structure"*** and ***"computer function".*** ***(20 marks)***

ii. Write down three (03) methods that can be used to assess the performance of the PC. ***(06 marks)***

iii. Briefly explain the three (03) key concepts of **Von Neumann Architecture**. ***(10 marks)***

b)

i. Briefly explain the purpose of a **Register** is. ***(04 marks)***

ii. Write down four (04) examples of **registers in the CPU**. ~~***(06 marks)***~~ (04 marks)

iii. Name four (04) main steps of the **Instruction Cycle** and briefly describe them. ***(12 marks)***

c)

i. What is **an Interrupt** in Computing? ***(08 marks)***

ii. Write down two (02) Advantages and two (02) Disadvantages of **Interrupts**. ***(04 marks)***

iii. Explain what is a **Computer Bus**. ***(06 marks)***

iv. Name three (03) types of computer buses. ***(06 marks)***

v. Define the terms "*Functional Dedication*" and "*Physical Dedication*". **(20 marks)**

2.

a)

i. Briefly explain what is **cache memory**. ***(10 marks)***

ii. List down two (02) advantages and two (02) disadvantages of **Cache Memory.** ***(04 marks)***

iii. Define the "***Temporal locality***" and "***Spatial Locality***" of reference. ***(20 marks)***

iv. Name four (04) types of **scheduling**. ***(04 marks)***

v. Name two (02) types of **partitioning** in memory management. ***(02 marks)***

b)

i. Name three (03) **mapping functions**. Briefly explain one of them. ***(14 marks)***

ii. Explain what **memory management** is in computer architecture. and discuss why it is important ***(10 marks)***

c) Consider a memory system that uses a 32bit address to address at the byte level and a cache that uses a 64-byte line size. Assuming an associative cache, draw the address format and determine the following parameters. ***(36 marks)***

i. Number of addressable units.

ii. Number of blocks in main memory.

iii. Size of the tag.

3.

a)

i. Briefly define the **RAID (Redundant Array of Independent Disks)** ***(10 marks)***

ii. List down two (02) physical characteristics of **(Magnetic Disks) disk systems.** ***(10 marks)***

iii. Compare the **SRAM (Static RAM)** and **DRAM (Dynamic RAM) with two(02) facts.** ***(12 marks)***

iv. Name two (02) **errors** in semiconductor memory systems. ***(02 marks)***

b)

i. Calculate the check bits for the data word 1011 using the hamming error correction code. Fill in the bit position, position number, and data bits and check for the given data word in Table 01. ***(14 marks)***

Table 1

Bit position	7	6	5	4	3	2	1
Position number							
Data bits							
Control bits							

C1=D1⊕D2⊕D4

C2=D1⊕D3⊕D4

C3=D2⊕D3⊕D4

ii. Draw the **Venn diagram** corresponding to the check bits for the given data word in 3) b) i).***(10 marks)***

c)

i. Briefly describe the following terms. ***(20 marks)***

a. Write Through

b. Write back

ii. Name two (02) **integer representations** in computer arithmetic ***.(02 marks)***

iii. Calculate the following using the 4–bit **signed magnitude notation**.

(10 marks)

a. (+4) + (+3)

b. (-4)+(-3)

iv. Carry out the following addition and subtraction using the 4-bit **1's complement notation**.

(10 marks)

a. (+5)+(+2)

b. (-5)+(-2)

4.

a) Simplify the following expression using **Boolean algebraic laws and rules. Clearly mention the laws and rule you follow.** ***(20 marks)***

$$M = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + AB\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D}$$

b) Draw the truth table for following **logic gates.** ***(20 marks)***

i. **XOR gate**

ii. **XNOR gate**

iii. Draw the **logical circuit diagrams** that implement the following expressions. ***(20 marks)***

a. $Y=\overline{AB(C+D)}$

b. $Y=\bar{A}B+\overline{C}$

c)

i. Briefly describe **Immediate addressing mode** and **Direct addressing mode** using appropriate diagrams. ***(20 marks)***

ii. Write down one (01) advantage each for **immediate addressing and direct addressing.** ***(08 marks)***

Immediate addressing	Direct addressing

iii. Name three (03) types of **Pipeline Hazards.** ***(03 marks)***

iv. Write down the purpose of having **resource hazards.** ***(09 marks)***

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