University of Ruhuna - Faculty of Technology

Bachelor of Engineering Technology

Level II (Semester II) Examination, September 2020

Course Unit: ENT2213 Digital Electronic Systems

Time Allowed 3 Hours

All symbols have their usual meaning

This question paper consists of 5 questions and 12 pages. Attach page 11 and 12 of this question paper to the answer script. All questions must be answered. All answers to new questions should start in a new page, and all the answers to each question should be organized together.

1)

I.

a) Show how do you convert the two decimal numbers 86 and 75 to Binary Coded Decimal (BCD) and 8-bit binary forms.

b) Show how do you convert the two negative decimal numbers -86 and -75 to 2's complement binary form.

c) Do the following additions and subtractions in their binary form and leave the final answer in binary form. Indicate if there is an overflow error. (Show your work)

i. 86 + 75

ii. 86 - 75

[50 marks]

II. An elevator is used for transportation between three floors (F1, F2, F3) in a three storied building. A logic circuit is used to control the operation of elevator door. The circuit has **four Boolean inputs and one output** as shown in Figure 1. Description of each input and output are given below.

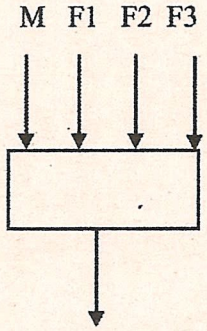

Figure 1

M is a logic signal that indicates whether the elevator is moving (M = 1) or stopped (M = 0).

F1, F2, and F3 are floor indicator signals that are normally LOW. They go HIGH only when the elevator is positioned at each floor 1,2, and 3 respectively. (For example, when the elevator is lined up with the second floor, F2 =1 and F1 = F3 = 0)

The circuit **output Y** is the DOOR OPEN signal, which is normally LOW and will go HIGH when the elevator door is to be opened.

a) Construct a truth table for above scenario. (Hint: Consider the cases where more than one floor input (F1, F2, F3) is HIGH as don't care conditions, since the elevator cannot be lined up with more than one floor at a time)

b) Draw the Karnaugh map for the door OPEN signal output.

c) Find the SOP (Sum of products) Boolean expression for the door OPEN signal using the Karnaugh map.

d) Draw the logic circuit for the above Boolean expression.

[50 marks]

2)

I.

a) Draw the logic symbol, truth table and write Boolean expression of the two input NAND gate and two input NOR gate.

b) Describe the first and second De Morgan's theorems which are used to find equivalent logic expressions for NAND and NOR gates. For two Boolean valued input variables A and B, express the above theorems using Boolean expressions.

[20 marks]

II. A logic circuit has three inputs A, B, and C and output Y. Output Y goes HIGH only when majority of the inputs are HIGH. The truth table for this scenario is shown below.

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

a) Write the SOP (Sum of Products) expression for the output Y using the above truth table.

b) Simplify the above SOP expression using Boolean algebra laws and rules.

[20 marks]

III.

a) Draw the equivalent logic circuit using NAND gates to the following logic gates.

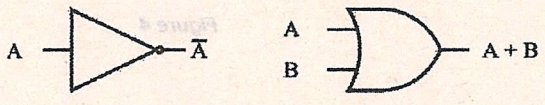

Figure 2

b) Draw the equivalent logic circuit using NOR gates to the following logic gates.

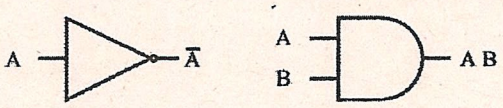

Figure 3

[30 marks]

IV.

a) Draw the logic circuit for the combinational logic function $F = (\bar{A} + B)(C + D)$ using AND, OR and NOT gates.

b) It is required to implement the above combinational logic using a **minimum number of Integrated Circuit (IC) packages** due to a space constraint in the circuit. A list of available IC packages and their pinout diagrams are shown in Figure 4. Redraw the logic circuit in part a) so that the number of IC packages used is minimized. Indicate the number of each IC package required for the design.

IC Package	Description
74LS00	Quad two input NAND gate
74LS02	Quad two input NOR gate
74LS04	Hex Inverter gates
74LS08	Quad two input AND gate
74LS32	Quad two input OR gate

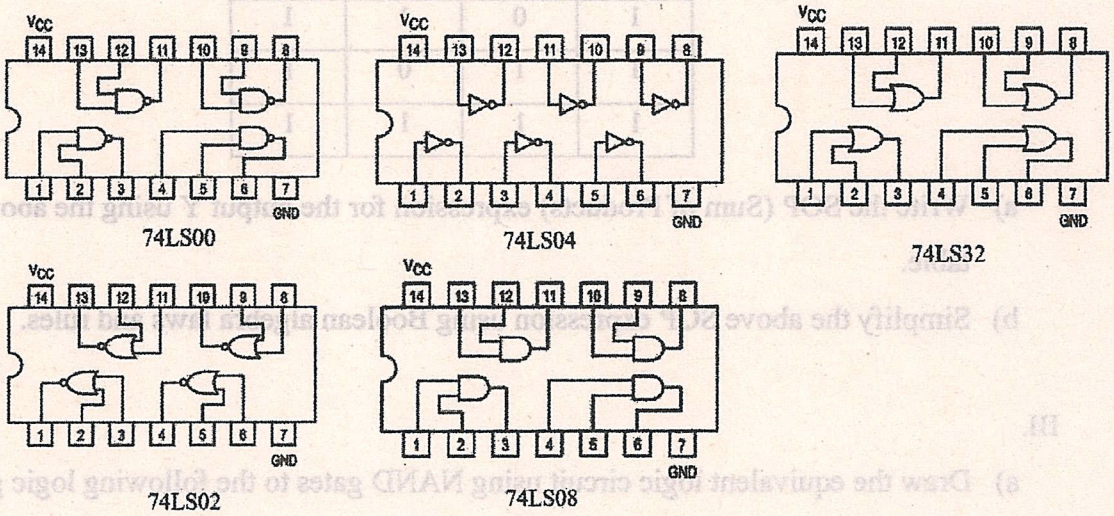

Figure 4

[30 marks]

3)

I. A 4 to 1 multiplexer has four data inputs (D0, D1, D2, D3), two select inputs (S1, S2) and one output (Y) as shown in Figure 5. All the input D's and S's can only take Boolean values.

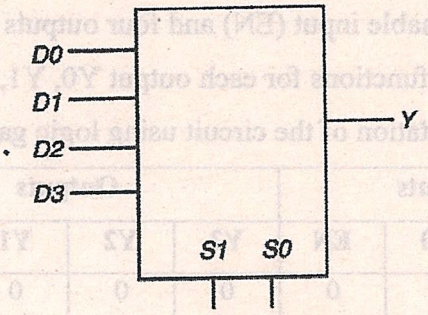

Figure 5

a) Construct a truth table for the above 4 to 1 multiplexer in the below format.

S1	S0	Y

b) Write a Boolean expression for the output (Y) in terms of inputs D's and S's.

c) Draw the corresponding logic circuit diagram for above expression for Y.

[50 marks]

II. Given below is a simplified Boolean expression which requires many separate logic gates to implement it. In this situation, a multiplexer can be used to generate this logic function. Show how the following Boolean function can be implemented using an 8 to 1 multiplexer and NOT gates.

$$Y = \overline{A}\,\overline{B}\,\overline{C} + A\,\overline{C}\,\overline{D} + \overline{A}CD + BC\overline{D} + \overline{B}CD$$

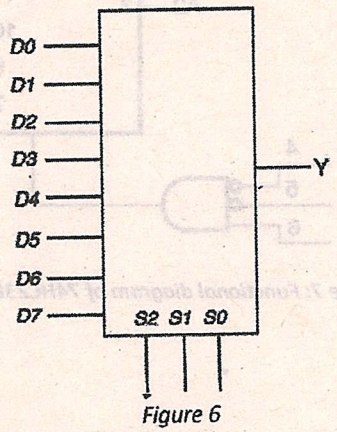

Figure 6

[50 marks]

4)

I.

a) Describe the function of a decoder.

b) Truth table of a 2-to-4-line decoder is given in the table below. The decoder has two data inputs (A0, A1), enable input (EN) and four outputs (Y0, Y1, Y2, Y3).

i. Write the decoding functions for each output Y0, Y1, Y2 and Y3.

ii. Draw the implementation of the circuit using logic gates.

Inputs			Outputs			
A1	**A0**	**EN**	**Y3**	**Y2**	**Y1**	**Y0**
×	×	0	0	0	0	0
0	0	1	0	0	0	1
0	1	1	0	0	1	0
1	0	1	0	1	0	0
1	1	1	1	0	0	0

[40 marks]

II. It is required to decode a 5 bit binary number ($A_4\,A_3A_2A_1A_0$) to control a certain operation of a digital circuit. 74HC238 is the available decoder and the above requirement should be achieved using these 3-to-8 line decoders and any other logic gates necessary.

Functional diagram, pin description and truth table of 74HC238 are shown below.

a) How many output levels can be controlled using 5 bits?

b) Make correct interconnections between the 3-to-8 line decoders given in page 11 to design a 5 bit decoder and attach it to your answer script. Clearly label the output pins.

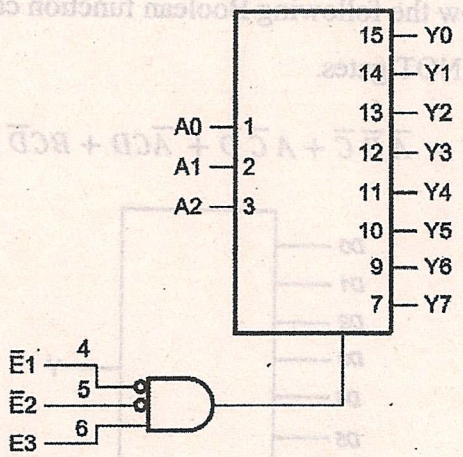

Figure 7: Functional diagram of 74HC238

Symbol	Pin	Description
$A0, A1, A2$	1,2,3	Address input
$\bar{E}1, \bar{E}2$	4,5	Enable input (active LOW)
$E3$	6	Enable input (active HIGH)
$Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7$	15,14,13,12,11,10,9,7	Output
GND	8	Ground (0 V)
V_{CC}	16	Supply voltage

Pin description of 74HC238

Inputs						Outputs							
$\overline{E1}$	$\overline{E2}$	$E3$	A0	A1	A2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

Truth table of 74HC238

[60 marks]

5)

I. Logic circuit diagram of a JK flipflop is shown in Figure 8.

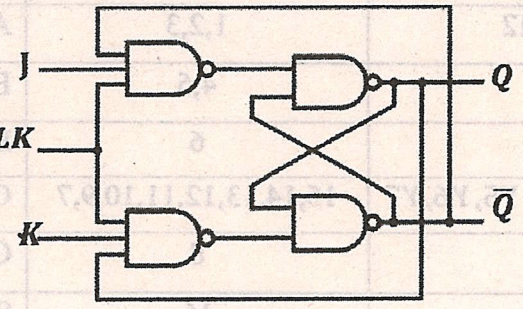

Figure 8

a) Modify the above logic circuit diagram to form an edge triggered JK flipflop.

b) Give the truth table of a positive edge triggered JK flipflop.

c) Draw the timing diagram of the output (Q) of a positive edge triggered JK flipflop for the given J, K and Clock inputs as shown in Figure 12 in page 12. The flipflop is initially Reset. Use the given space in page 11 to draw the output (Q) and attach it to your answer script.

[20 marks]

II. A 4-bit shift register is shown below in Figure 9.

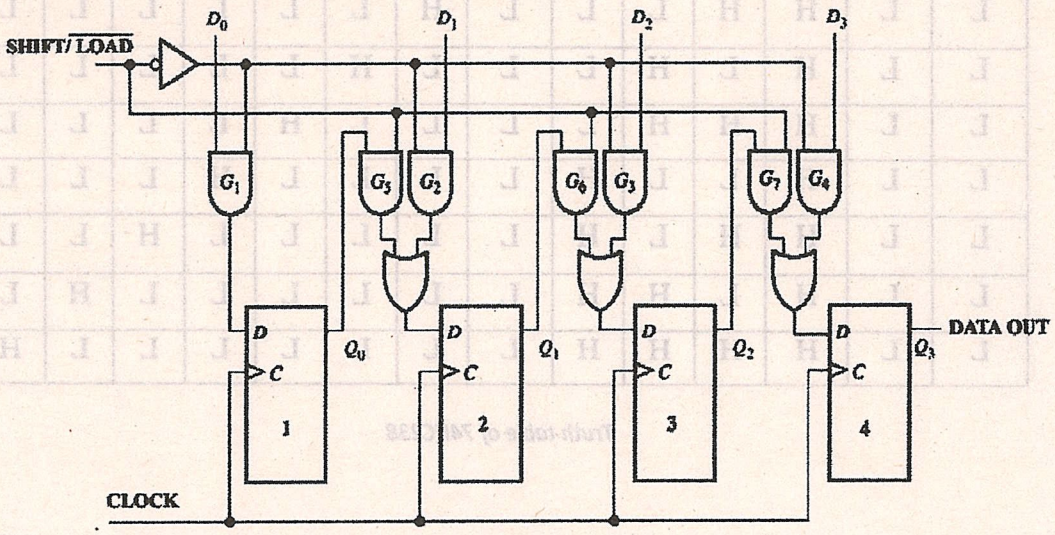

Figure 9

a) Identify the type of this shift register.

b) If $D_0 = 0, D_1 = 0, D_2 = 1, D_3 = 1$, show the data-output waveform for this shift register when the Clock and $SHIFT/\overline{LOAD}$ waveforms are applied as in Figure 13 shown in page 12. Assume the register is initially Reset. Use the given space to draw the waveforms in page 11 and attach it to your answer script.

[20 marks]

III.

a) Copy the diagrams to your answer script and show how to form a modulus 8 **(MOD 8) asynchronous binary down counter** by making the correct connections between the given negative edge triggered JK flipflops in Figure 10.

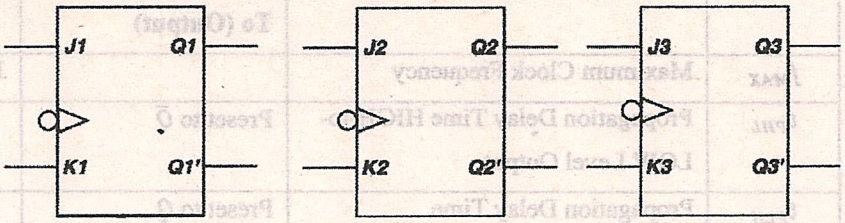

Figure 10

b) For the above counter,

i. Write the three-bit binary counting sequence in a table. Clearly indicate the output pin name ($e.g\ Q1/\overline{Q1}$) which corresponds to each bit.

ii. For ten Clock pulses, draw the timing diagrams for Clock input and output of each for above counter. Assume all the flipflops are initially in Reset. Clearly label each diagram with the relevant output pin name ($e.g. Q1/\overline{Q1}$).

iii. Calculate the frequency at the output of the last flipflop, given that the Clock frequency is 2MHz.

iv. What will be the counter's state after 97 Clock pulses, given that all the flipflops are initially Reset?

[40 marks]

IV. Shown below is a specification table extracted from a manufacturer's datasheet for a 7476 J-K Flip-Flop. Calculate the maximum decimal number that can be reliably counted using these flipflops.

Symbol	Parameter	From (Input) To (Output)	Min	Max	Units
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\bar{Q}$		28	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		24	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q		28	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\bar{Q}$		24	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\bar{Q}$		28	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\bar{Q}$		24	ns

[20 marks]

INDEX NO:

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5. I) c)

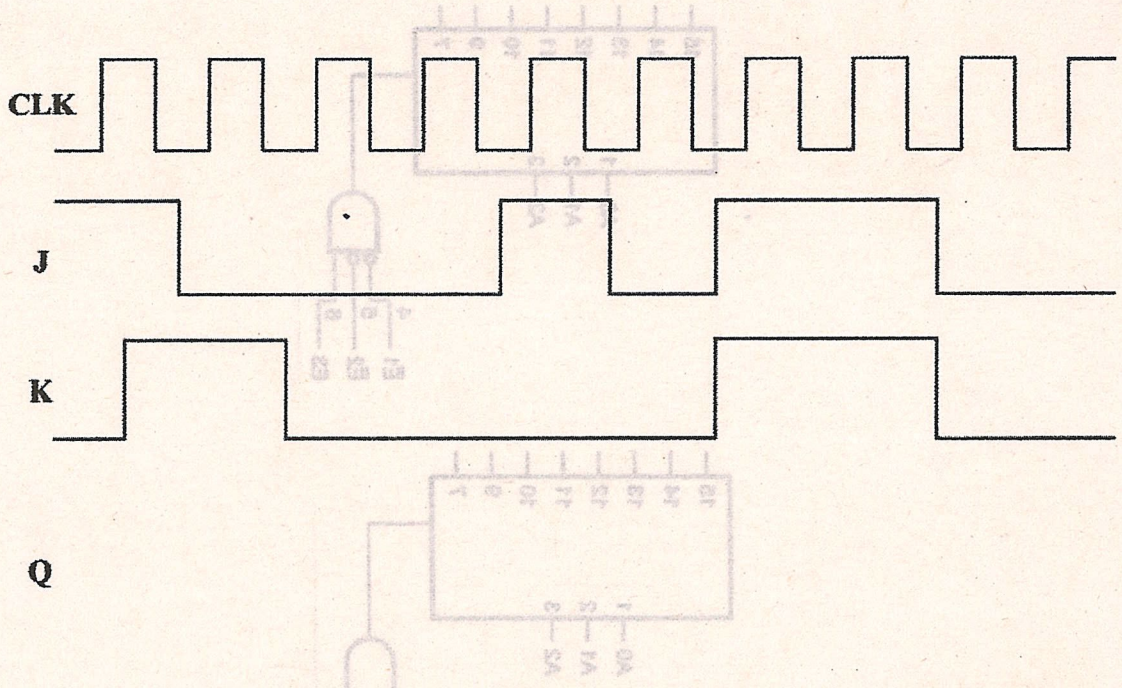
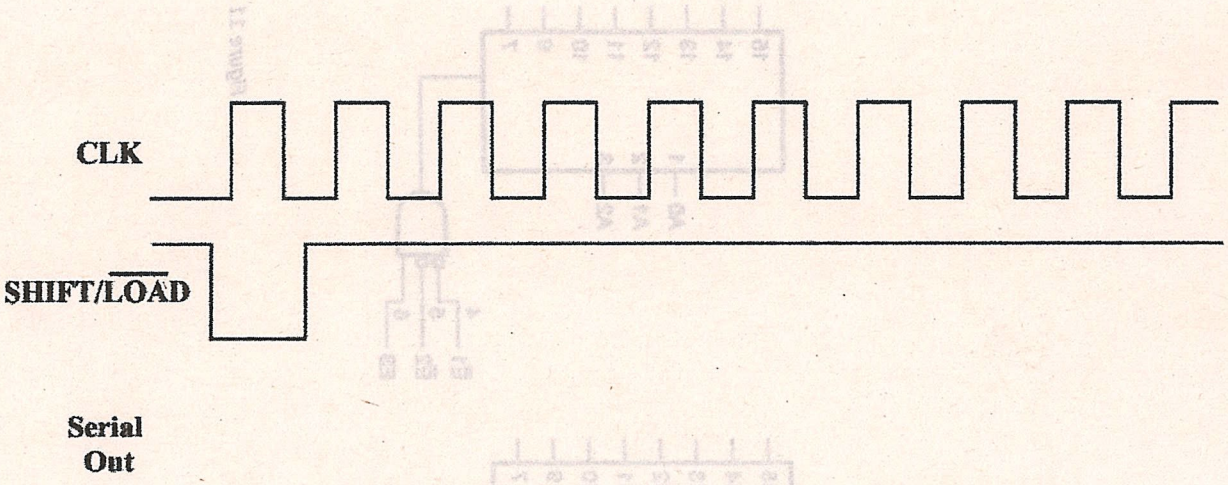


Figure 12

5.II) b)



Serial Out

Figure 13

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3. II) b)

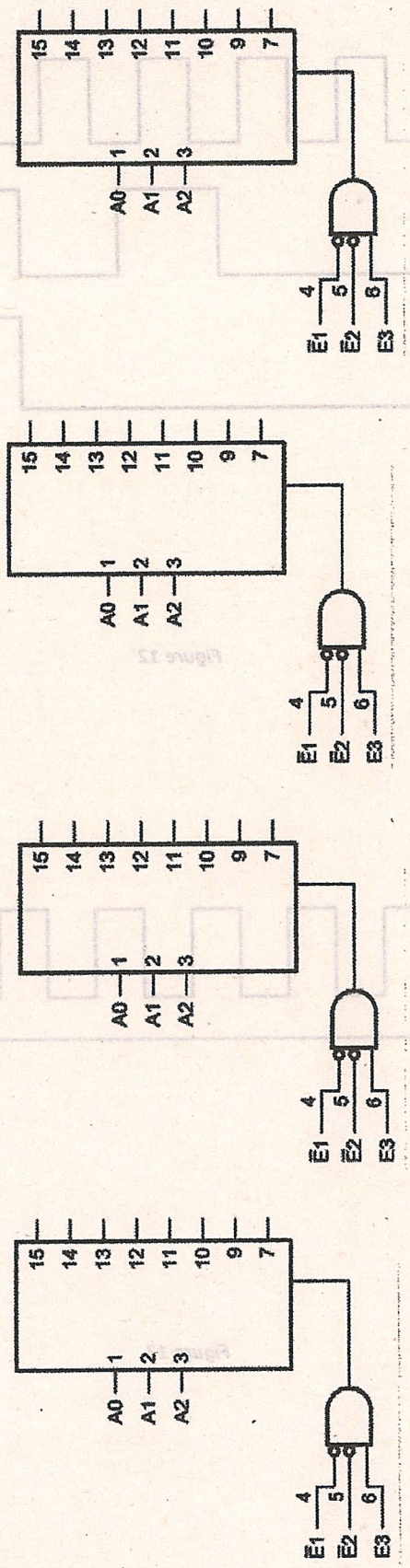

Figure 11

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5. I) c)

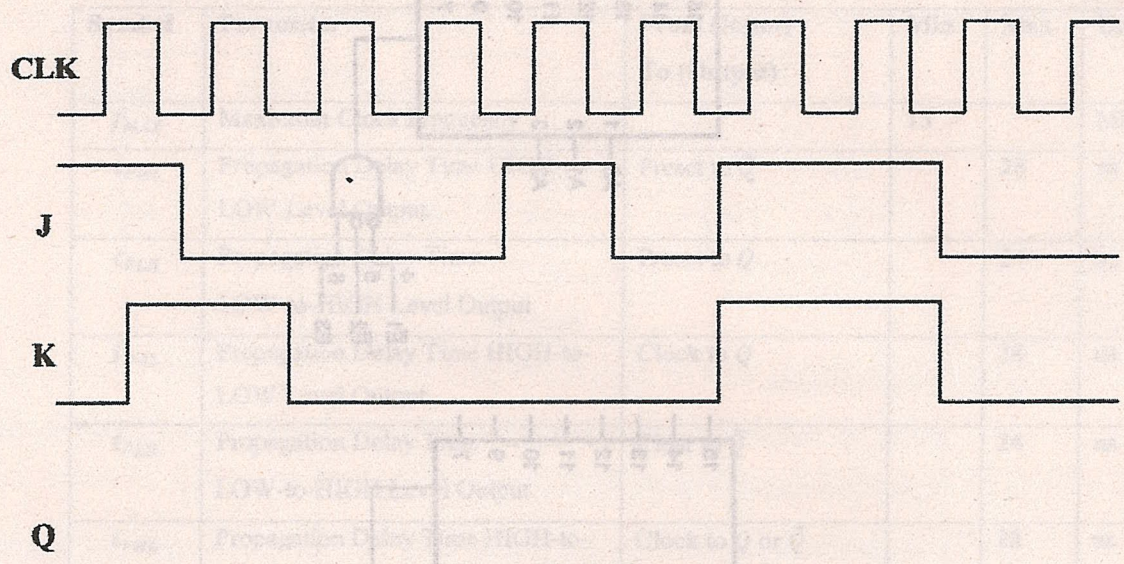

Figure 12

5.II) b)

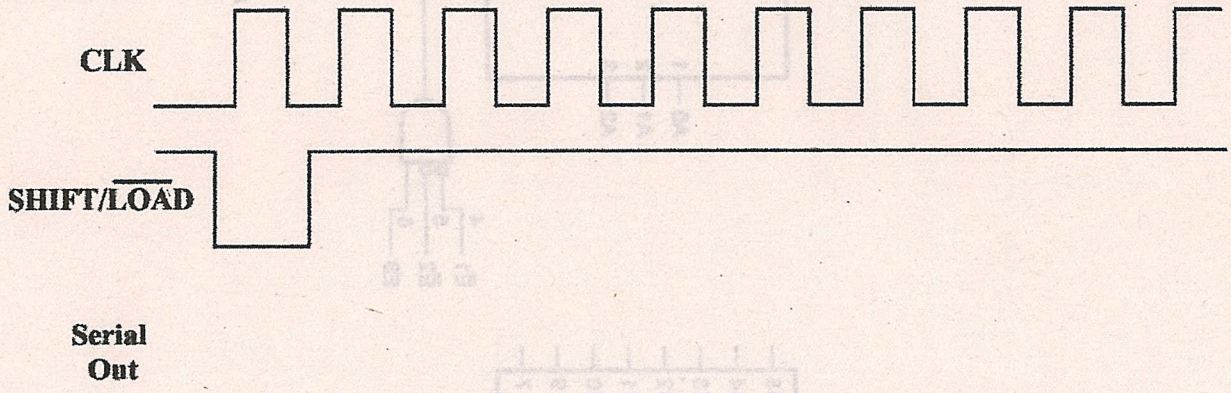

Figure 13