UNIVERSITY OF RUHUNA
BACHELOR OF COMPUTER SCIENCE (GENERAL) DEGREE
LEVEL II (SEMESTER II) EXAMINATIONS
NOVEMBER/DECEMBER – 2016

Subject: Computer Science
Course unit: CSC2222 (Computer Systems II) **Duration: 2 hours**

Answer All Four (4) Questions

1)

a) What are the three main components of the computer, when we consider the top level view of the computer?

b)

I. Show the two main steps of the instruction cycle using a diagram.

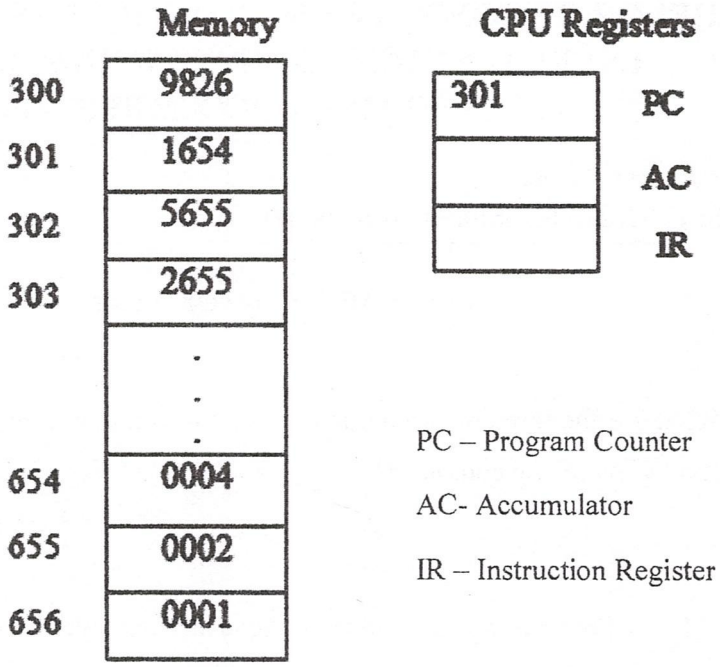
II. What is the purpose of the program counter?

c) The main function of the computer is executing instructions. The following diagram shows the states of the memory and CPU registers before executing an instruction. Clearly show the steps of adding content of memory location 654 to content of memory location 655. Both instructions and data are 16 bits long.

You have to use the following list of op codes.

0001 – Load AC from memory
0010 – Store AC to memory
0101 – Add to AC from memory

Continue



d) Consider a main memory system that uses a 64-bit address to address at the byte level. Assume an associative cache which uses a 32-byte line size

I. What is meant by associative mapping?

II. Show the address format of the main memory.

III. Determine the number of addrressable units and number of blocks in main memory

Continue

2)

a)

I. System buses can be classified into three functional groups. What are they?

II. What is the difference between functional dedication and physical dedication in the bus architecture?

b)

I. What is meant by an interrupt in a computer system?

II. Briefly describe the two methods, which are used to handle multiple interrupts.

c)

I. Name the two ways of representing an integer? Give **a** drawback **or** a benefit for each representation.

II. Subtract -63 from 69 using two's complement representation. (Use 8 bits to represent numbers). Is there overflow? Justify your answer.

III. Use the appropriate algorithm and multiply -12(multiplicand) by 5(multiplier). (Represent each number using 5 bits)

3)

a)

I. In magnetic disk, the substrate can be constructed using Aluminum or glass. Name three benefits of using glass instead of Aluminum.

II. In RAID architecture how many levels are in common use? What are the **three** common characteristics of RAID levels (except in level 0)?

Continue

b)

I. Name two improved versions of DRAM

II. Write two differences and two similarities of EPROM and EEPROM.

c)

I. Name two types of errors which can occur on semiconductor memory types?

II. Suppose there is an 8-bit data word. In order to perform single bit hamming error correction how many check bits are required?

III. If the 8 bit data word which is stored in memory is equal to 11001110, calculate the check bits which are required to store in memory with the data word. Display the bit position, position number, data bits and check bits using a table for the given data word (Hint: least significant data bit = first data bit).

IV. After reading the word from the memory, if the calculated check bits are similar to 1011 in which bit position the error has occurred? What action should be taken by the system in such a situation?

4)

a)

I. State the 4 (four) elements of a computer instruction.

II. Name 2 (two) common **transfer of control** operations.

III. State 4 (four) design decisions in designing an instruction set.

b)

I. For the bit stream 011011100, perform **Logical right shift** and **Arithmetic Left Shift** 3 (three) times.

II. Using suitable diagrams, briefly describe **Immediate Addressing** mode and **Direct Addressing** mode. (Your diagram should show the format of the instruction and the location of the operand).

c)

I. Draw the structure of a register window used in RISC architecture. Briefly describe the role of each area of a register window.

II. Explain how the register windows allow passing the data between procedures without moving data.

d) Assume a pipeline with four stages:

1. Fetch instruction (FI)
2. Decode instruction and calculate addresses (DA)
3. Fetch operand (FO)
4. Execute (EX)

Each stage mentioned above takes **10μs** time to complete the operation. Also, these all stages can be performed in parallel without any memory conflicts. For a sequence of five (5) instructions:

I. Sketch the timing diagram for instruction pipelining.

II. Using the timing diagram in (**I**), calculate the total time for execution of above five instructions under instruction pipelining.

III. Find the ratio between the time of execution **under instruction pipelining** and the time of execution **without instruction pipelining**.