

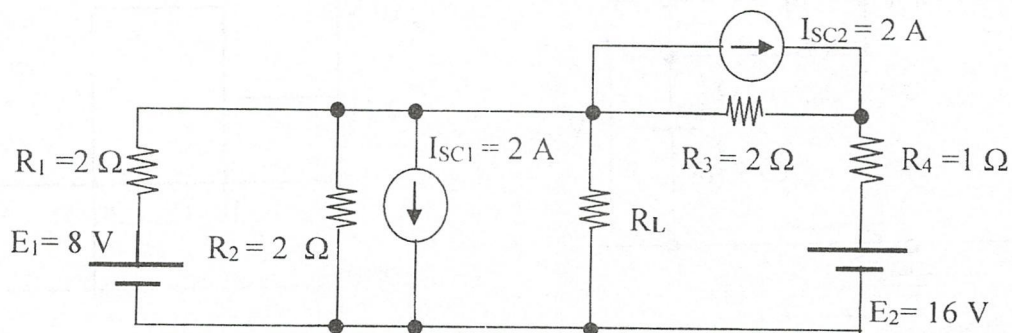
University of Ruhuna
Bachelor of Science (General) Degree Level II (Semester I) Examination
September -2017

Subject: Physics
Course Unit: PHY 2112

PART B - 01 hour & 15 minutes
Answer FIVE questions only.
All symbols have their usual meaning.

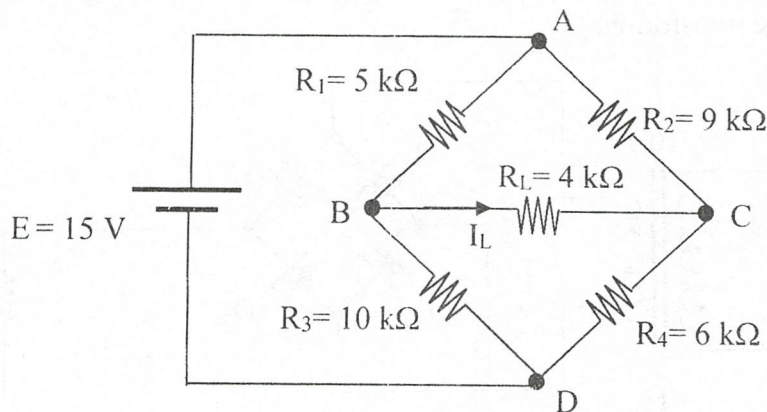
1.

(a) Consider the circuit shown below.



- i Using the source conversion calculate the thevenin's voltage across the R_L [4 Marks]
- ii What would be the maximum current passing through R_L ? [2 Marks]
- iii What would be the value of R_L in order to draw the maximum power from the circuit? [1 Marks]
- iv Calculate the maximum power drawn through the circuit by R_L . [1 Marks]

(b) Calculate the current (I_L) passing through the load resistor by using the Thevenin's theorem, in the circuit given below [2 Marks]



2. A capacitor of capacitance C and a resistor (R) is connected in series with a battery of e.m.f. E at time $t = 0$. The voltage across the capacitor, V_C , as a function of time t is given by,

$$V_C = V_0 e^{-\frac{t}{RC}} + E \left(1 - e^{-\frac{t}{RC}} \right) \quad \text{Where: } V_0 \text{ is the initial voltage of the capacitor}$$

(a) Sketch the variation of V_C as function of time for the following cases.

i $0 V < V_0 < E$ and

ii $0 V < E < V_0$

[1 Marks]

[1 Marks]

(b)

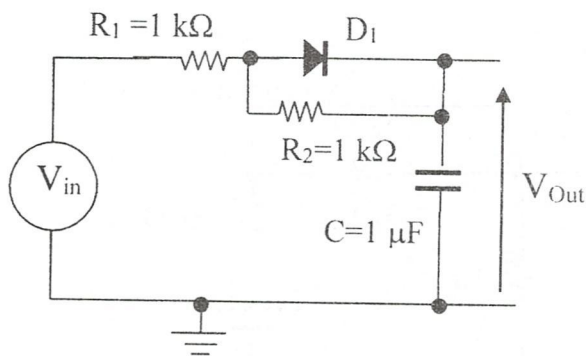


Figure A

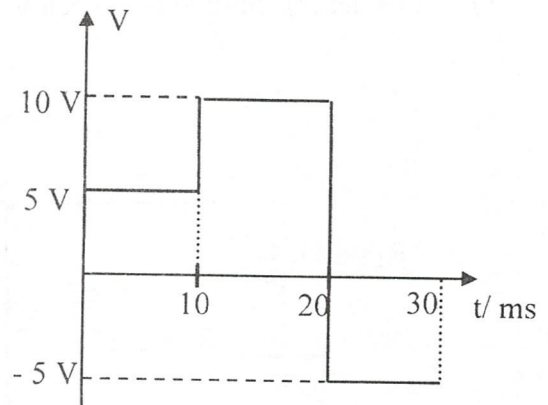


Figure B

Time dependent input voltage (V_{in}) shown in **figure B** is supplied to the circuit shown in **figure A**, which consists of two resistors, an ideal diode and an initially uncharged capacitor.

i Calculate the time constants for each voltage transitions

[1 Marks]

ii Sketch the variation of the output voltage (V_{out}) as a function of time, t for the period

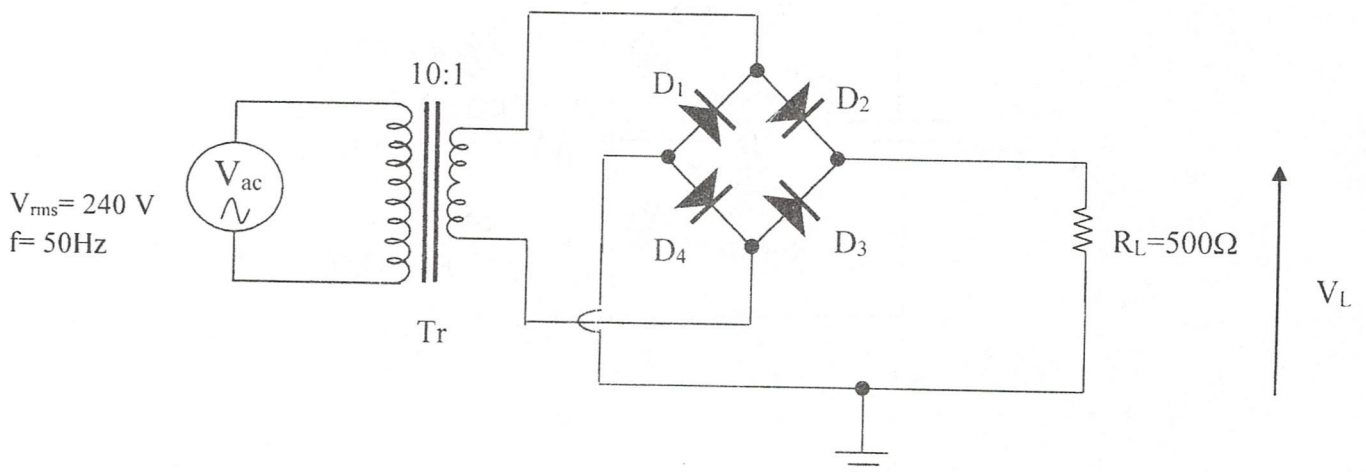
$0 \leq t \leq 30$ ms. (Assume that during each voltage transition capacitor stops the current conduction after a period of five time constants)

[4 Marks]

iii If the diode R_2 is open-circuited due to a fault, redraw the function in part **b (ii)**.

[3 Marks]

3. Answer the following parts considering the rectifier circuit given below. Neglect the resistance of the secondary winding of the transformer.



See the next page

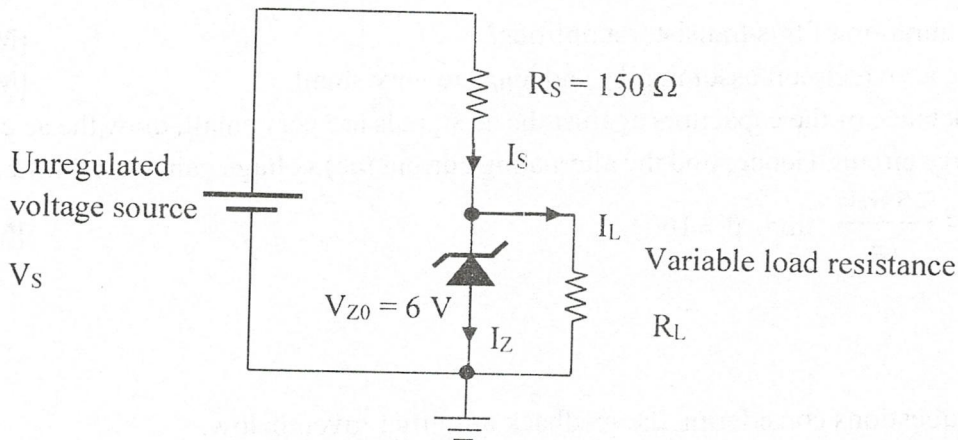
(a) Calculate the followings (considering all diodes are ideal)

- i Peak value of the voltage across R_L , [3 Marks]
- ii rms value of the voltage across R_L , [1 Marks]
- iii value of the d.c. component of the voltage across R_L and [2 Marks]
- iv value of the a.c. component of the voltage across R_L [2 Marks]

(b) If each diode has 0.7 V of forward bias voltage (V_{D0}), calculate the followings by using the constant voltage drop model for diodes

- i Peak value of the voltage across R_L , [1 Marks]
- ii Peak inverse voltage (PIV) of a diode [1 Marks]

4. Consider the following zener diode shunt voltage regulator circuit.



This circuit is working under the following conditions

Variable	Minimum value	Maximum value
V_s (unregulated voltage)	12 V	24 V
I_L (current through the load)	2 mA	35 mA

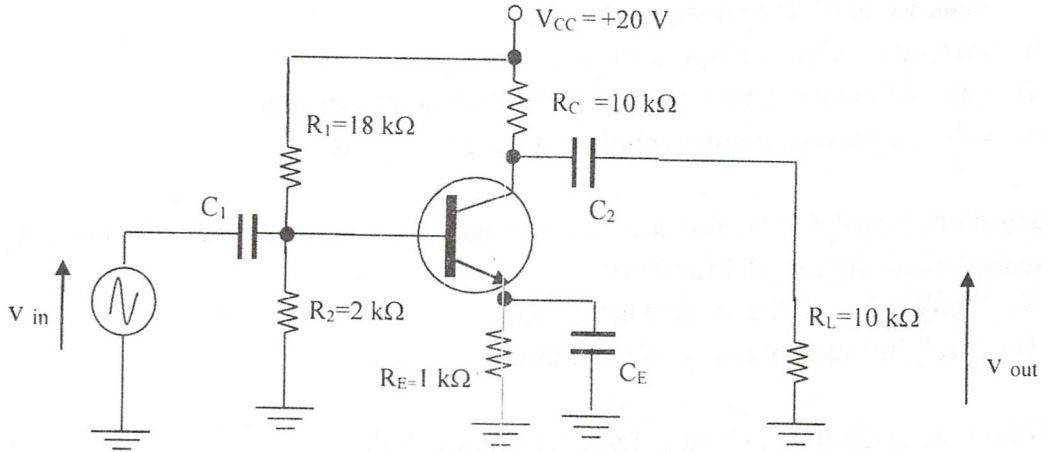
(a) Answer the following parts.

- i What is the desired regulated voltage across the load? [2 Marks]
- ii Assuming that this circuit operates as a voltage regulator, find the possible maximum and minimum current through the zener diode under the given conditions (use the constant voltage drop model for a zener diode). [4 Marks]

(b) If $P_{z(max)}$ is 750 mW and the minimum current ($I_{z min}$) of the zener diode to operate in the linear range is 2 mA,

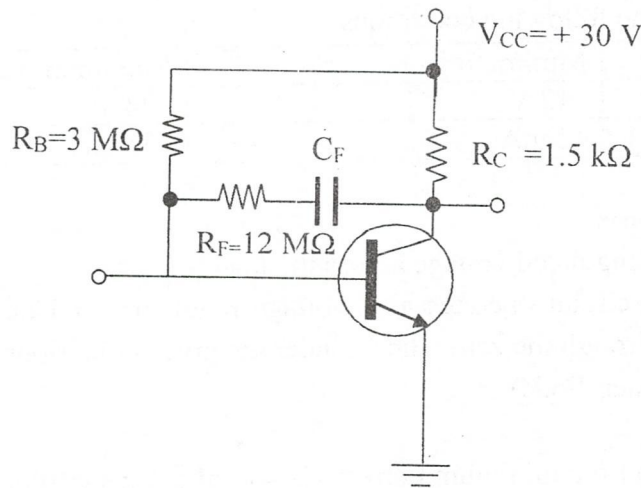
- i is it possible to operate this circuit as a voltage regulator under the variations mentioned above? [2 Marks]
- ii What would be the impact on the zener diode, when the maximum value of the unregulated voltage supply (V_s) is increased up to 50 V due to a fault? [2 Marks]

5. Consider the following amplifier circuit.



- (a) What is the configuration of this transistor amplifier? [Marks 2]
- (b) Calculate I_E of the above circuit assuming I_B and V_{BE} are very small. [Marks 3]
- (c) Assuming the reactance of the capacitors against the ac signals are very small, draw the ac equivalent circuit for the above circuit. Hence, find the alternating current (ac) voltage gain (take emitter intrinsic resistance, $r_e' = \frac{25 \text{ mV}}{I_E}$ and $\beta = 100$). [Marks 5]

6. Answer the following questions considering the feedback amplifier given below.



- (a) What is the form of the feed-back of this circuit? [2 Marks]
- (b) Calculate the following quantities. [take $r_e' = \frac{25 \text{ mV}}{I_E}$, common emitter current gain ($\beta = 100$) and V_{BE} is very smaller value]
- (i) Open-loop gain, [4 Marks]
- (ii) feed-back fraction and [2 Marks]
- (iii) closed-loop gain of the amplifier [2 Marks]

7.

(a) A logic circuit has three inputs (A, B, and C) and one output (Z). All input/output logic combinations of the circuit are shown in the following truth table,

A	B	C	Output Z
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

- i Derive a logic expression for output signal (Z) as a logic function of inputs. [2 Marks]
 - ii Simplify the logic expression obtained above. [2 Marks]
 - iii Construct a logic circuit by using the minimum number of 2-input NOR gates in order to implement the above logic expression. [3 Marks]
- (b) Simplify the following expression using a Karnaugh-Map (K-Map). [3 Marks]

$$X = \bar{B}. \bar{C}. \bar{D} + \bar{A}. \bar{B}. C. \bar{D} + A. \bar{B}. C. \bar{D}$$

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