UNIVERSITY OF RUHUNA
BACHELOR OF COMPUTER SCIENCE (GENERAL) DEGREE
LEVEL II (SEMESTER II) EXAMINATION – JANUARY 2018

CSC2222 – Computers Systems II **Duration: 2 hours**

Answer All Four (4) Questions

1.

a) Briefly explain what is meant by the **General Purpose Hardware Configuration** in **Von Neumann Architecture**.

b)

i. State **three (3)** classes of **interrupts**.

ii. Briefly explain the **two (2)** approaches of handling **multiple interrupts**.

c) What is the difference between **Centralized Bus Arbitration** and **Distributed Bus Arbitration**?

d) Consider a computer with following characteristics.

- **Size of memory address** : **32 bit**
- **Word size** : **32 bits (4 bytes)**
- **Block size** : **4 words (16 bytes)**
- **Cache size** : **64 Kbytes**.

i. If **direct mapping** is used in this cache, calculate the **Tag, Line** and **Offset** of the main memory address.

ii. If **four way set associative mapping** is used, find out where a word from the main memory location **ABCDE8F8** (in hexadecimal) is mapped in the cache.

iii. Name **two (2)** possible **Replacement Algorithms** that can be used for a cache using **four way set associative mapping**.

Continue...

2.

a)

i. State **three (3) nonvolatile semiconductor** memory types.

ii. What is the difference between **SRAM (Static RAM)** and **DRAM (Dynamic RAM)** in terms of the hardware technology of bit storage?

b) Briefly explain the advantage of using **SDRAM (Synchronous DRAM)** instead of **DRAM** in a CPU design.

c)

i. State the **two (2)** types of errors that can occur on **semiconductor** memory types.

ii. Calculate the **minimum** number of **check bits** required for **Single Error Correction** when the data word sizes are **8 bits** and **64 bits** respectively.

d) Answer the following questions assuming that **Hamming Code** algorithm is used for **Single Error Correction** in a memory with **8 bit** data words with **4 check bits**.

i. Fill the table given below and obtain the equations for check bit calculation.

Bit Position	12	11	10	9	8	7	6	5	4	3	2	1
Position Number												
Data bits												
Check bits												

ii. Using the equations obtained in **(d) (i)**, calculate the composite **code word** stored in the memory for the data word **00110011**.

iii. For the 8-bit data word **00111001**, the **check bits** stored with it would be **0111**. Suppose for a word read from memory, the check bits are calculated to be **1101**. What is the data word that was read from memory?

Continue...

3.

a)

i. Briefly explain how data are read and written in **Optical Storage** devices.

ii. Nowadays, the disk substrate of **magnetic disks** is created with **glass** rather than **aluminum**. State **three (3)** advantages of this usage.

b)

i. *"At least three disks need to fail for a data loss in RAID-6"*. Briefly explain the reason for this.

ii. Rotating disk at **constant angular velocity** wastes the space on **outer tracks** of magnetic disks. Briefly explain how this drawback is overcome in modern hard disks.

c)

i. Write down the **minimum** and the **maximum** integer that can be represented with **16 bits** using **Two's complement** binary number representation.

ii. Evaluate the following expression using **Computer Arithmetic** with **Two's complement** binary number representation. Name the algorithms or rules you use for this calculation.

$$((-14) \times 4) + 80$$

d) Explain how **(-5)** can be represented using **IEEE 32-bit** floating point format as given below.

Sign of significand (1 bit)	**Biased exponent** (8 bits)	**Significand** (23 bits)

Continue...

4.

a)

i. State **three (3)** types of **instructions** used in a computer system.

ii. Briefly explain the method of handling **procedure calls** with their parameters in processing of **Transfer of Control** operations.

b)

i. What is meant by a **True General Purpose** register?

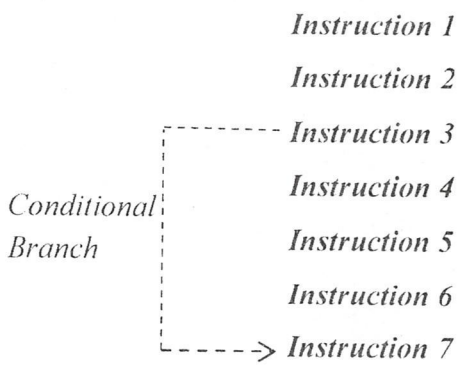
ii. Draw the structure and explain the role of each area of a **register window** used in **RISC (Reduced Instruction Set Computers)**.

iii. State **three (3)** differences between the usage of **large register files** and **caches** for quick accessing of operands.

c) An **Instruction cycle** consists of following **four (4)** steps.

I. Fetch Instruction (**FI**)
II. Decode Instruction and calculate address (**DA**)
III. Fetch Operand (**FO**)
IV. Execute (**EX**)

Each step mentioned above takes **5µs** to complete. Suppose there is a sequence of **seven (7)** instructions to be executed in a **pipeline**. Assume that the **third (3rd) instruction** is a conditional branch to the **seventh (7th) instruction** as shown in the following figure.



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Assume that all four steps of the instructions can be executed in parallel without any memory conflicts. If the **branch is taken** during the execution in the pipeline mode:

i. Draw the timing diagram for instruction pipelining of the above sequence of instructions.

ii. Using the timing diagram in **(c) (i)**, calculate the total time for the execution of given sequence of instructions under **instruction pipelining.**

iii. Find the ratio between the time of execution **under instruction pipelining** and the time of execution **without instruction pipelining**.

d) What is meant by **Pipeline Hazards**?