UNIVERSITY OF RUHUNA

BACHELOR OF SCIENCE SPECIAL DEGREE LEVEL I (Semester II)
EXAMINATION DECEMBER- 2017

Subject: PHYSICS
Course unit: PHY4112, Electronics II **TIME: 02 hours**

Answer FOUR (04) questions only

Q1.

a) Design a logic circuit that has three inputs, A, B and C, and which will produce HIGH output only when two or more inputs are HIGH.

[07 marks]

b) In an audio CD, the audio voltage signal is typically sampled about 44,000 times per second, and the value of each sample is recorded on the CD surface as a binary number. The each recorded binary number represents a single point on the audio signal wave form.

i. If the binary numbers are six bits in length, how many different voltage values can be represented by a single binary number? Repeat for eight bits and ten bits.

ii. If ten-bit numbers are used, how many bits will be recorded on the CD in one second?

iii. If a CD-ROM can store 650 megabytes, how many seconds of audio can be recorded when ten-bit numbers are used (mega $=2^{20}$).

[09 marks]

c) The movement of binary data and codes from one location to another is the most frequent operation performed in a digital system.

i. What is the major cause of error in transmission process?

ii. Why this error is significant?

iii. Briefly discuss the parity method in detecting the error code.

[09 marks]

Q2. Digital systems obtain binary coded data and information that are continuously being operated on in some manner like decoding and encoding, multiplexing and demultiplexing etc.

i. What are the functions of decoder and encoder?

ii. Discuss an application of a priority encoder.

iii. Using Karnaugh map or other method design logic circuit diagram for 4-input priority encoder (4 to 2 line priority encoder).

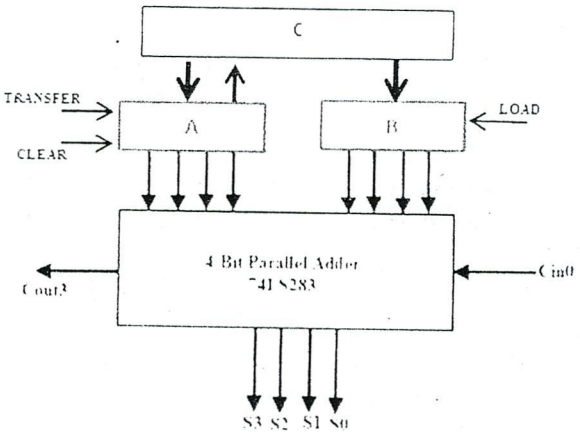
iv. What are the functions of multiplexer and demultiplexer?

v. Giving relevant gate combinations explain the function of a circuit of two-input multiplexer.

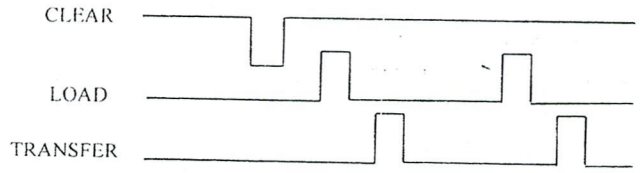
[25 marks]

Q3.

Several parallel adders are available as ICs. The most common is four-bit parallel adder, illustrated in the figure. All the bits of A and B are fed into the adder circuits simultaneously and therefore parallel addition is very fast.



i. Construct logic circuit diagram for a single bit full adder circuit.
ii. What are A, B and C circuits of the given full adder?
iii. Write down the sequence of operation of the complete adder by following the given timing diagram.

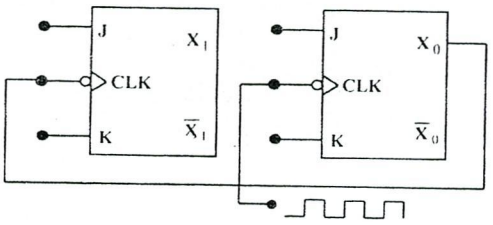


iv. What is the main cause of delay in an adder circuit and what remedy has been used in this circuit to overcome the delay?
v. Draw necessary modification to perform subtraction operations using the same circuit.

[25 marks]

Q4.

Clocked flip-flops are versatile devices that can be used in variety of applications including frequency division and counting. Figure shows the wiring arrangement of two J-K flip-flops to form a two bit binary counter.



a)

i. Extend the flip-flop arrangement for 3-bit asynchronous (ripple) up counter.
ii. What is meant by up counters and down counters and what changes has to be taken to convert this to down counter?
iii. By drawing all waveforms explain the operation of a 3-bit up counter.
iv. Write down all possible counting operations for 3-bit up counter.
v. Modify the same counter to perform the counting operations only between 2 and 5.

[18 marks]

Continue to next page..

b)

i. Design a logic circuit for 3-bit synchronous up counter.
ii. "Counting operations of synchronous counters are stable than asynchronous counters". Explain this statement briefly.

[07 marks]

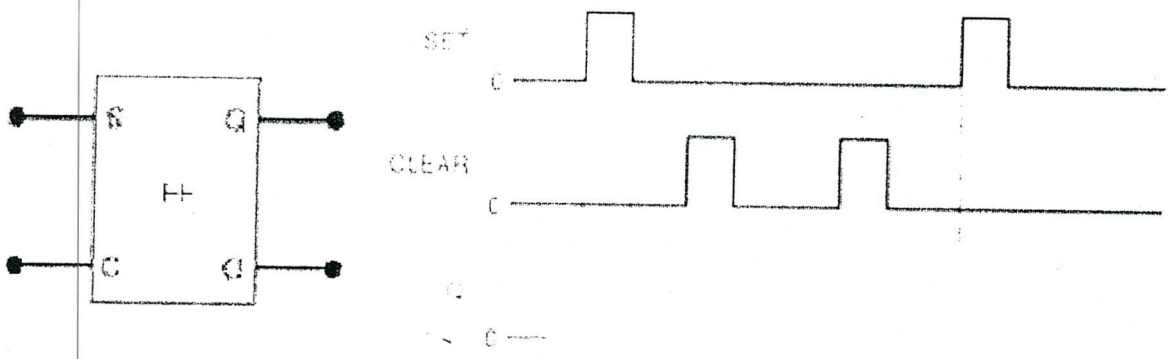
Q5.

a) Discuss **any two** of the following Flip-Flop applications.
   i. Flop-Flop synchronizations
   ii. Detecting the input sequence
   iii. Serial data transfer

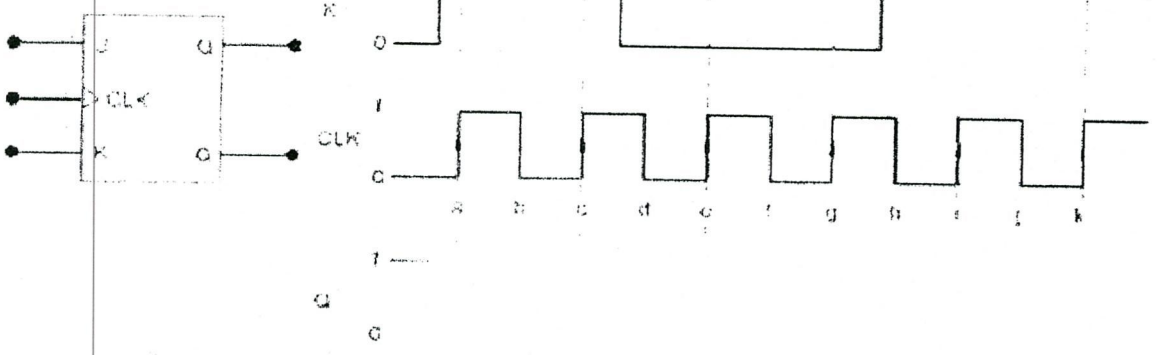
[05 marks]

b) Use same sheet to answer this question and attached with your answer scripts. Complete the output wave forms of given flip-flops (i to v) according to their inputs.

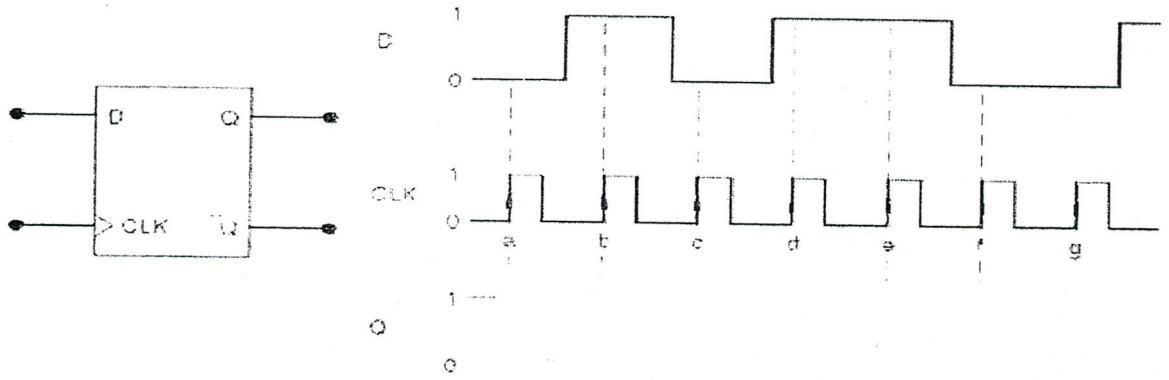
i.



ii.



iii



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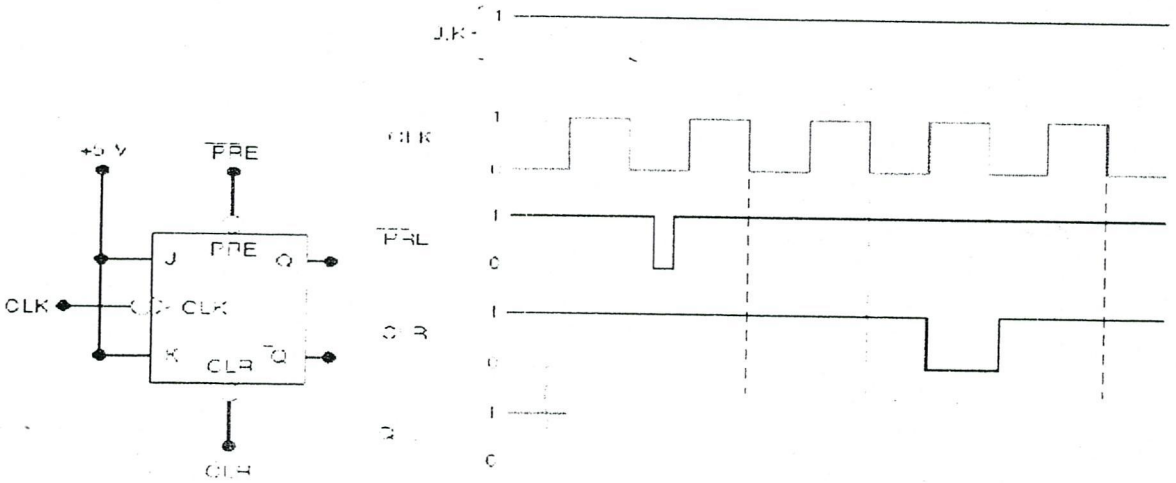
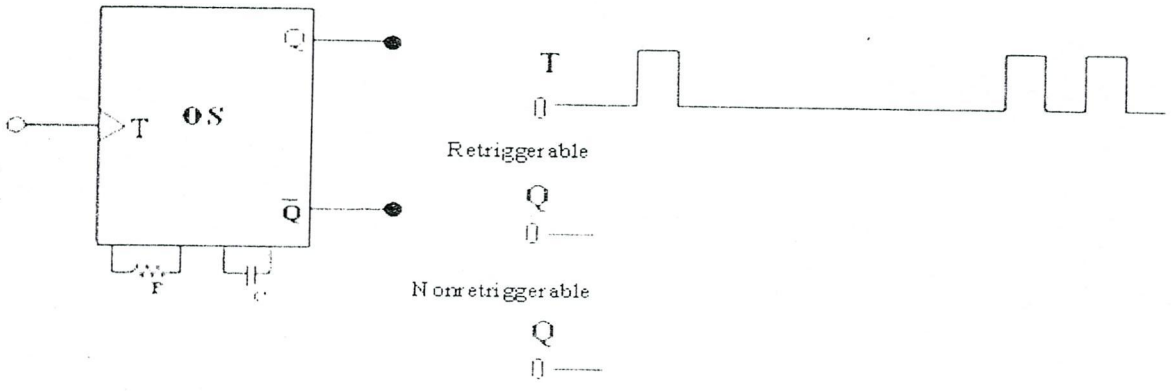


v



(Note: Quasi stable interval is 2 ms (> width of the clock pulse) for **both cases)**

[20 marks]