UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 2 Examination in Engineering: February 2020

Module Number: EE2202 **Module Name: Introduction to Electronic Engineering**

[Three Hours]

[Answer **all questions**, each question carries **10 marks**]

All notations have the usual meaning.

Q1 a) Simplify the following Boolean equations using the Karnaugh map.

i) $Z = (\overline{A}\overline{B} + AB)\,\overline{C} + \overline{A}B + AC$

ii) $Z = (\overline{A}\overline{B} + A\overline{B})\,(\overline{C}\overline{D} + C\overline{D})$

iii) $Z = (\overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C)(D + \overline{D}) + B(\overline{C}\overline{D} + C\overline{D}) + A\overline{B}\overline{D}\,(C + \overline{C}) + A\overline{B}D$

[5 Marks]

b) Figure Q1 b) shows a representative circuit of an amplifier with a source of voltage v_s and internal resistance r_s connected to a load R_L. The voltage and current gains of the amplifier are A_v and A_i respectively.

i) Give equations for the overall voltage gain (v_L/v_s) and the overall current gain (i_L/i_s).

ii) Based on the equations in part b) i), state the desirable conditions for a voltage amplifier and a current amplifier to have no reduction in the overall gain.

iii) For a matched source and load, show that the overall power gain is ($A_vA_i/16$).

[5 Marks]

Q2 a) Figure Q2 a) shows the bias circuit for a Silicon Bipolar Junction Transistor (BJT) with $\beta = 100$. Find the bias (Q) point of the transistor.

[1.5 Marks]

b) State and verify that the rule for biasing the transistor is satisfied by the circuit.

[1.5 Marks]

c) Sketch the typical output characteristics for a BJT biased as in Figure Q2 a). Clearly name the axes and the units, and identify the different regions of operation.

[2 Marks]

d) Modify the circuit in Figure Q2 a) for the transistor to act as a switch (inverter) and explain its operation.

[2.5 Marks]

e) i) Give the BJT transistor circuits for logic gates AND and OR.

ii) Give the equivalent circuits for part e) i) in terms of the transistors acting as switches and verify the operation with truth tables.

[2.5 Marks]

Q3 a) Figure Q3 a) shows the AC equivalent circuit for a Bipolar Junction Transistor. r_i and r_o are the input and output resistances respectively.

i) For the transistor in Common-Base (C-B) configuration, define r_i and r_o, and give an explicit expression to determine r_i.

ii) Starting from the C-B amplifier circuit, use the AC equivalent circuit for the transistor to show that the voltage gain $A_v = (R_c/r_e)$ and current gain $A_i = \alpha$.

iii) For the transistor in Common-Emitter (C-E) configuration, derive an expression for r_i and then give an expression for r_o by inference.

iv) Starting from the C-E amplifier circuit, use the AC equivalent circuit for the transistor to show that the voltage gain $A_v = (-R_c/r_e)$ and the current gain $A_i = \beta$.

v) Based on the above results, explain why the C-E amplifier is better suited as a voltage amplifier.

[7 Marks]

b) Give the Common-Collector amplifier circuit and its AC equivalent, and show that its voltage gain $A_v \approx 1$.

[3 Marks]

Q4 a) Sketch the structure of a biased N-type Junction Field Effect Transistor (JFET), and identify the terminals, the channel and the biasing voltage sources V_{DS} and V_{GS}.

[1.5 Marks]

b) i) Sketch the formation of the depletion regions for $V_{DS} = 0$, $V_{GS} \neq 0$.

ii) Sketch the formation of the depletion regions for $V_{GS} = 0$, $V_{DS} \neq 0$.

iii) Explain the difference in shape of the depletion regions in parts b) i) and ii).

[1.5 Marks]

c) An N-type JFET has a pinch off voltage $V_P = (-4)$ V and a saturation current $I_{DSS} = 12$ mA.

i) Construct a table of V_{DS} (sat) and I_D for $V_{GS} = 0$ to (-4) V in (-1) V steps, and sketch the Drain characteristics.
Note: $V_{DS} = V_{GS} - V_P$ and $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$

ii) From the Drain characteristics, construct the Transfer characteristics for the JFET.

[2 Marks]

d) i) State the meaning of the acronym MOSFET and give the circuit symbols for a depletion type N-MOSFET and P-MOSFET.

ii) Sketch the structure of a biased depletion type N-MOSFET and show the terminals, the channel and the bias voltage sources V_{DS} and V_{GS}.

iii) Explain how the depletion type N-MOSFET can be used in the enhancement mode.

iv) Sketch the typical Drain characteristics for the depletion type N-MOSFET operating in the depletion and enhancement modes.

[5 Marks]

Q5 a) i) Give the circuit of a Cross-NOR S-R Flip-Flop.

ii) Explain its operating conditions and construct the function table.

iii) The S-R input waveforms for this Flip-Flop is shown in Figure Q5 a). Synthesize the Q and $\overline{Q}$ output waveforms.

[3 Marks]

b) i) Reconstruct the circuit of a Master-Slave J-K Flip-Flop based on two S-R latches.

ii) Explain the Toggle operating mode for this Flip-Flop.

[3 Marks]

c) i) Explain the difference between pulse triggered and edge-triggered J-K Flip-Flops.

ii) Give the circuit symbols for the two types of edge-triggered J-K Flip-Flops.

iii) Give the circuit diagram for a MOD-8 Ripple Counter based on three negative edge-triggered J-K Flip-Flops.

iv) If a clock pulse is given for a Ripple Counter as shown in Figure Q5 c), synthesize the waveforms for the three outputs.
Note: Neglect the zero counter input.

[4 Marks]

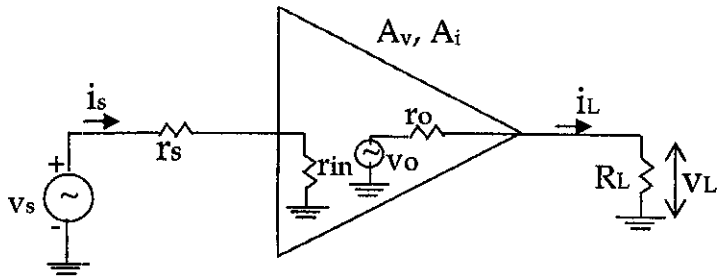

Figure Q1 b): Representative circuit of an amplifier with the source and load

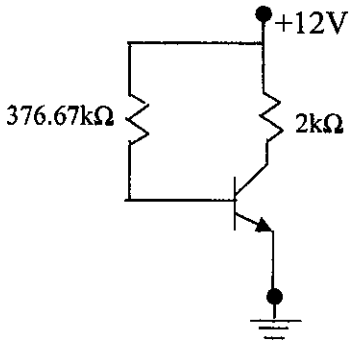

Figure Q2 a): Bias circuit for a Silicon BJT

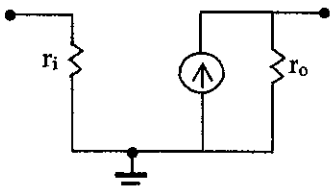

Figure Q3 a): AC equivalent circuit for a BJT

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Use this page for answers to Q5 a) and Q5 c) and attach it to your answer script.

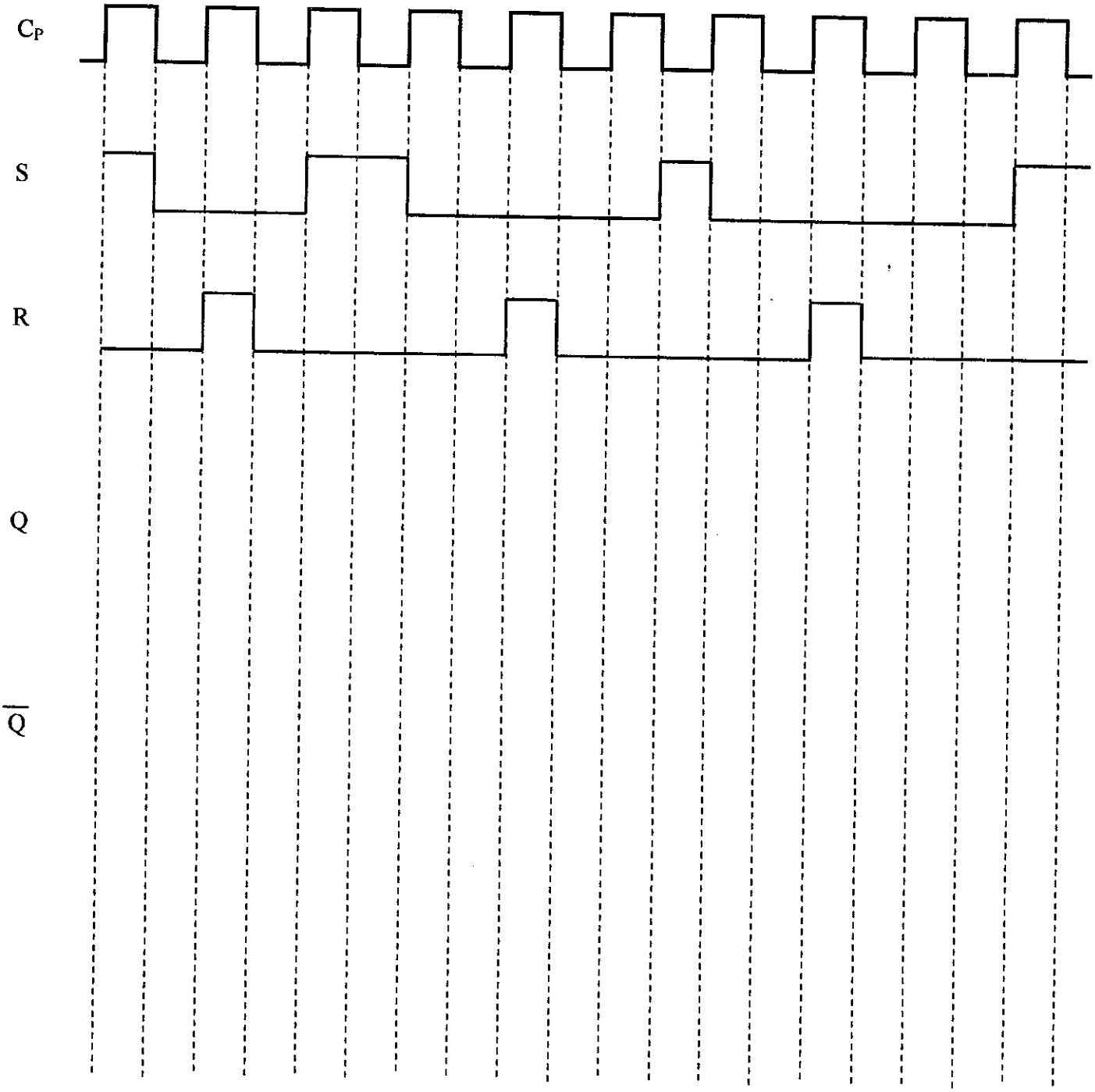

Figure Q5 a)

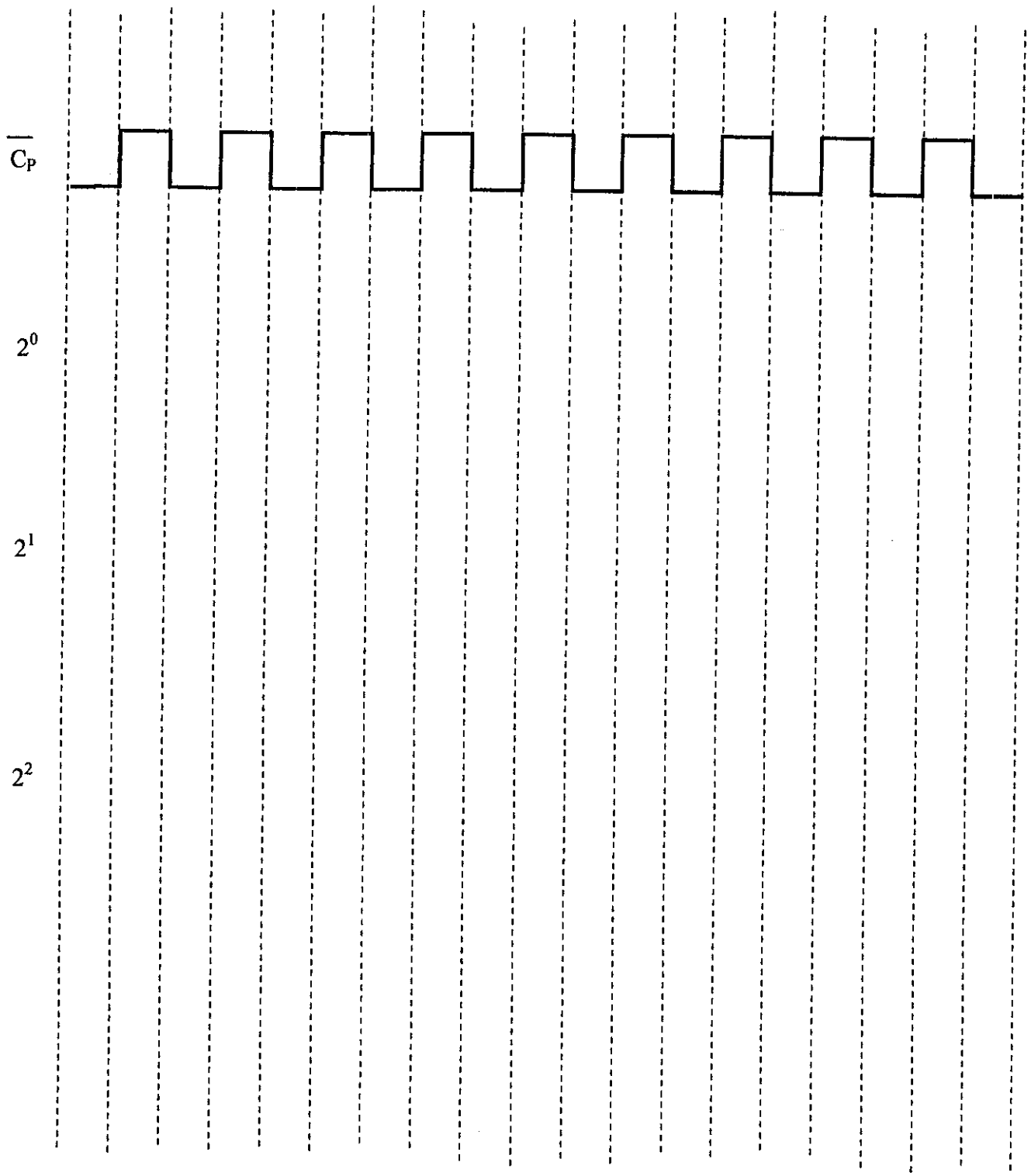

Figure Q5 c)