UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 4 Examination in Engineering: February 2020

Module Number: EE4302 Module Name: Digital Electronics

[Three Hours]

[Answer **all questions**, each question carries 10 marks]

Q1 a) Assume that you were to minimize a logic function F(A,B,C,D) using the Quine-McClusky method and ended up with the result given in Table 1.1.

i) Identify the Prime implicants and complete the Table 1.1

ii) Using the Prime implicants in part i), identify the essential prime implicants clearly showing the steps.

[3 Marks]

b) Consider the two K-maps for output F1 and F2 as given in Figure 1.1.

i) Write the minimized logic function for F1

ii) Write the minimized logic function for F2 in terms of F1.

[2 Marks]

c) A 2-bit equality comparator is shown in Figure 1.2 that compares the two-bit binary numbers A_1A_0 with B_1B_0. The output F is True only when $A_0 = B_0$ and $A_1 = B_1$ both happens at the same time (i.e. when $A_1A_0 = B_1B_0$).

Given a 4-bit binary number $X_3X_2X_1X_0$, we need to find a given 2-bit target pattern Y_1Y_0 appear within $X_3X_2X_1X_0$.

For example:
if $X_3X_2X_1X_0$ = 0110 and the target pattern Y_1Y_0 = 10, the target pattern appears once within $X_3X_2X_1X_0$ at 0^{th} and 1^{st} bit positions;

if $X_3X_2X_1X_0$ = 1000 and the target pattern Y_1Y_0 = 00, the target pattern appears twice within $X_3X_2X_1X_0$ at 0^{th}, 1^{st} bit positions and 1^{st}, 2^{nd} bit positions.

i) Draw a pattern detector to detect the availability of a given 2-bit pattern within a 4-bit number using one or more 2-bit equality comparators shown in Figure 1.2 and required logic gates. Clearly name the inputs and the outputs.

ii) Change your circuit to a pattern counter which counts the frequency of occurrence of a two bit number within a four bit sequence. Draw the circuit using one or more 2-bit equality comparators shown in Figure 1.2 and required logic gates. Clearly name the inputs and outputs.

Hint: identify the maximum possible occurrences of the target pattern, decide on the required number of output bits, and derive the required logic functions for each output bit.

[5 marks]

Q2 a) Write the excitation tables for D type and T type FlipFlops.

[1 Mark]

b) The state transition diagram of a synchronizer is illustrated in Figure 2. User input is denoted by r, and synchronizer state is denoted by $S_2S_1S_0$ (001, 010, and 100).

i) Write the state transition table.

ii) Identify the state assignment technique used in this synchronizer.

iii) Determine the logic equation for each FlipFlop input to implement the synchronizer circuit using D FlipFlops.

[5 Mark]

c) You have to design a Garage door opener/closer panel with two push buttons, Open button (S) and Close button (C). Its functionality is specified as follows.

- When the system is powered on for the first time, it will be idling. That is, neither opening nor closing the door.
- If Open button is pressed while door is idling or closing, door will start opening.
- If Open or Close button is pressed while door is opening, door will stop opening (back to idle).
- If Close button is pressed while door is idling, door will start closing.
- If Open or Close button is pressed while door is closing, door will stop closing (back to idle).
- If both buttons are pressed together, the input will be ignored.

In order to open the door, a motor M_S will be activated and to close the door, a motor M_C will be activated.

i) Identify the inputs and outputs of the system.

ii) Implement a simple Moore machine for the garage door opener panel.

iii) Use the sequential state assignment technique to assign the states.

[4 Marks]

Q3 Consider the logic circuit in Figure 3 that has two outputs.

a) Obtain the logic equation for each of the outputs Y1 and Y2.

[1 Mark]

b) Derive the flow table using the equations obtained in part a).

[2 Marks]

c) Identify if there is a raise condition and name the state and the input.

[1 Mark]

d) i) Name if there are static hazards.

ii) Do the necessary changes to the logic equations of Y1 and Y2 to remove them.

[2 Marks]

e) i) Write down the excitation table for the RS latch.

ii) Determine the input logic functions for each of the inputs if we are to implement the circuit using two RS latches.

[4 Marks]

Q4 a) List unipolar and bipolar logic families (two from each category)

[1 Mark]

b) State the key advantage of Emitter coupled logic (ECL) over Transistor-transistor Logic (TTL) and briefly explain the reason

[2 Marks]

c) Give one key reason for you to choose CMOS logic family to implement a circuit over the TTL logic family?

[1 Mark]

d) Draw a simple CMOS logic circuit to implement $F(A,B) = \overline{(A+B)}$

[1 Mark]

e) Consider the TTL logic network in Figure 4. The inputs A, B, C, and D are applied +5 V to make them 'HIGH' or connected to ground to make them 'LOW'. All eight transistors are of the type NPN and Vo is the output voltage.

i) Considering a transistor as being active at saturated mode/ as logical 1 and inactive at cutoff mode/ as logical 0, identify the logic function for transistor Q3, giving reasons.

ii) Derive a logic function for the output Vo in terms of the inputs A, B, C, and D giving reasons.

iii) If R1 = 2 kΩ and R2 = 1 kΩ, what is the current through R2 when Vo is 'LOW'. Clearly mention your assumptions on junction voltages of the transistors.

[5 Marks]

Q5 a) Comment on the stability of a digital filter in which the transfer function is $h[n] = \tan[n]\ U[n]$.

[1 Mark]

b) Determine the type of frequency response of the filter given by

$$y[n] = 1.1\, x[n] + 0.4\, x[n-1] - 0.3x[n-2] + 0.4\, x[n-3]$$

[1 Mark]

c) Consider the digital filter in which the output is

$$y[n] = x[n] + 2x[n-1] + x[n-2] + 1.7y[n-1] - 0.6y[n-2].$$

i) Evaluate the transfer function of the filter.

ii) Comment on the causality and stability of the filter.

iii) Draw a block diagram for the filter.

[4 Marks]

d) Consider a bandpass filter with the transfer function $H_d(\omega)$ which is to be designed using the frequency sampling method where,

$$H_d(\omega) = \begin{cases} e^{-j4\omega} & \frac{\pi}{3} < |\omega| < \frac{3\pi}{4} \\ 0 & elsewhere \end{cases}.$$

i) Identify the number of frequency samples to be used and the frequency sampling interval.

ii) Evaluate the transfer function.

$$\text{Hint: } h_d[n] = \frac{1}{2M+1}\left(H_d(\omega_0) + \sum_{k=1}^{M} H_d(\omega_k)(e^{-jn\omega_k} + e^{jn\omega_k})\right)$$

[4 Marks]

Table 1.1

Group	Minterms	Binary
G1'	m4, m5, m12, m13	x 1 0 x
	m4, m12, m5, m13	x 1 0 x
G2'	m3, m7, m11, m15	x x 1 1
	m3, m11, m7, m15	x x 1 1
G3'	m3, m7, m13, m15	x 1 x 1
	m3, m13, m7, m15	x 1 x 1

Note: x denotes either 1 or 0

AB / CD	00	01	11	10
00	1	1	0	0
01	0	0	1	0
11	0	0	1	0
10	1	1	0	0

F_1

AB / CD	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	1	1	0	1
10	0	1	1	1

F_2

Figure 1.1

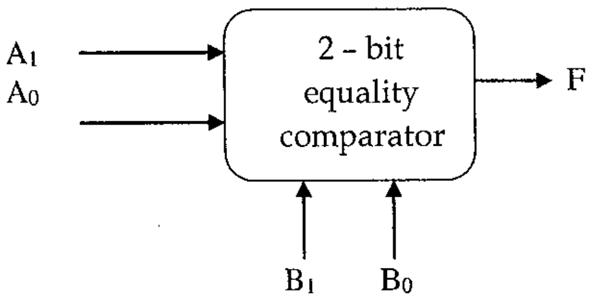

Figure 1.2

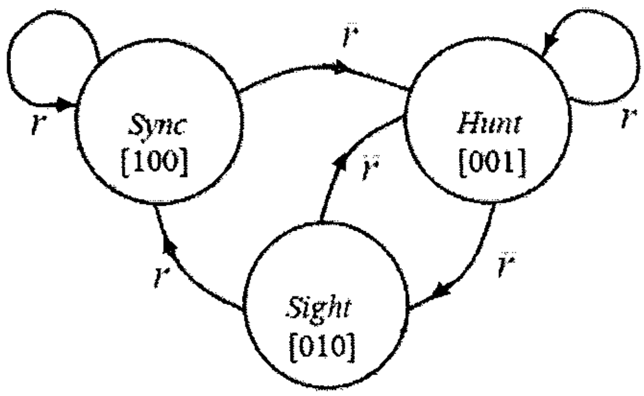

Figure 2

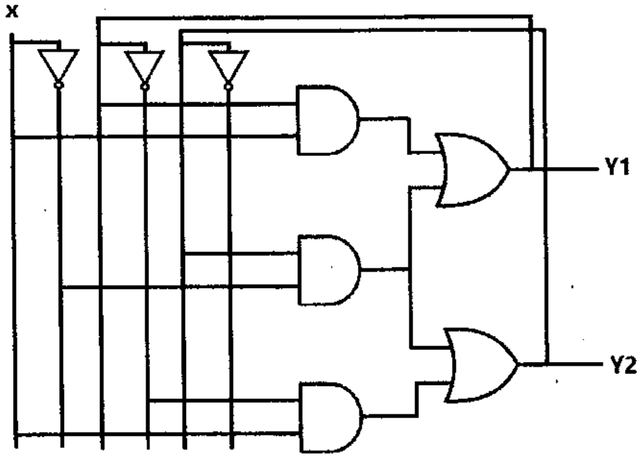

Figure 3

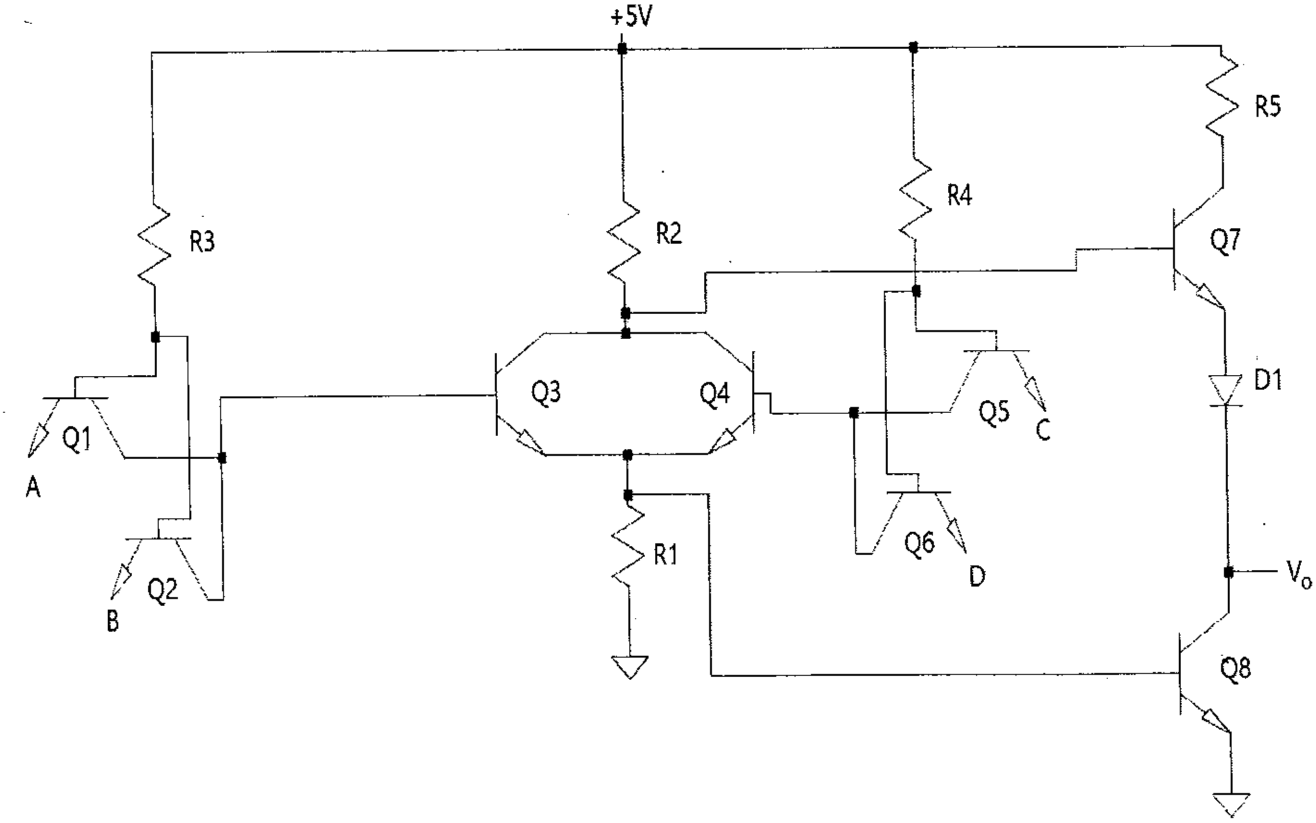

Figure 4