UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 6 Examination in Engineering: February 2020

Module Number: EE6208 **Module Name: Introduction to Hardware Description Languages**

[Three Hours]

[Answer all questions, each question carries 10 marks]

Q1 a) A half-subtractor is used to subtract one binary digit from another to give a DIFFERENCE output and a BORROW output.

i) Write a Verilog code to create a half-subtracter referring to the logic implementation and the Boolean expression of a half-subtracter shown in Figure Q1 a) i).

ii) Implementation of a full-subtractor using logic gates is shown in Figure Q1 a) ii). Re-using the half-subtractor created in part a) i), write a Verilog code to create a full-subtracter.

iii) Using the full-subtractor crated in part a) ii), design a 4-bit subtractor providing a diagram of a logic implementation and a Verilog code.

[5.0 Marks]

b) i) The input to a Finite State Machine (FSM) is a sequence of binary bits in series. Design a FSM which recognizes the bit pattern "111".

Hint:
When the FSM sees three 1's in a row, it should generate logic "1", otherwise "0".

ii) Write a Verilog code for the FSM designed in part b) i) if a positive edge of a clock drives the input data and the output.

[5.0 Marks]

Q2 a) i) What is a Hardware Description Language (HDL)?

ii) Explain the importance of HDL in digital system designing.

iii) Give four examples of HDLs used in designing and verification of digital systems.

iv) What are the basic HDL abstraction levels used in chip designing? Briefly explain each abstraction level.

[5.0 Marks]

b) Model a "memory" using Verilog HDL (Register Transfer Level design) by considering the following criteria.

- Size of the memory is 8 bits wide and the address space is 64.
  Reg [7:0] mem[0:63];
- The memory is addressable via a 5 bit address bus.
  input [5:0] address;
- An Enable pin (input) to enable the memory. When the memory is not enabled, pass a high impedance value.
  dataOut = 8'bz;

- "ReadWrite" is an input pin where the value decides whether the operation is a Read operation or a Write operation.
  ReadWrite = 1 //Read operation
  ReadWrite = 0 //Write operation
- "dataIn" and "dataOut" are input and output ports to write to the memory and read from the memory, respectively.
- Comment on relevant locations to explain the operation.

Directions: Use the following template to implement your code.

```
module memory (//Your inputs and outputs go here);
reg [7:0] mem[0:63];
//Your code
endmodule
```

[4.0 Marks]

c) What is a Verilog testbench and how it differs from a Verilog design?

[1.0 Mark]

Q3 a) i) What is a Clock Domain Crossing (CDC) in a synchronous digital circuit?
ii) Explain the Setup time and the Hold time in a Filp-Flop (FF).
iii) What are the causes of Setup/Hold time violation?
iv) State one harmful impact that occurs in a design due to the metastability and discuss how to prevent that.

[4.0 Marks]

b) The main function of a synchronizer is to mitigate the effect due to metastability. The most common synchronizer used by designers is two Flip-Flop (2-FF) synchronizer. Mostly the control signals (qualifiers) in a design are synchronized using 2-FF synchronizers.
i) Describe the functionality of a qualifier in CDC synchronizers.
ii) Indicate the valid qualifiers and the blocking values relate to schematic diagrams given in Table Q3 b). Note that, CLK1 and CLK2 are asynchronous clocks for flip-flops.
(Redraw the table in your answer sheet without "Schematic Diagram" column and indicate the responses.)

[4.0 Marks]

c) Can the circuit diagram given in Figure Q3) c) stop the metastability? Justify your answer.

[2.0 Marks]

Q4 a) i) State the name used to describe a current flow from a power rail to a ground rail through partially biased transistors.
ii) Suggest two methods to reduce dynamic/active power in Application Specific Integrated Circuits (ASIC).
iii) Recognize the languages used in the snippets shown in Figure Q4) a) iii (1) and Figure Q4) a) iii (2) respectively.

[5.0 Marks]

b) A small power domain architecture is shown in Figure Q4 b) and its power state table is given in Table Q4 b).

i) State whether isolation cells and/or level shifter cells are needed to be inserted in each path P1 and P2.

ii) What are the types of level shifter cells to be inserted in paths P1, P2 and P3 if required?

iii) Give one example where "always-on buffers" are used.

[5.0 Marks]

Q5 Power estimation plays a critical role in ASIC design. Knowing the potential power consumption of the design before fabrication is important to make sure whether the end product is feasible and to find any potential bugs in the design. The power of a chip is determined by calculating the dynamic and static power components of the design.

a) i) Briefly explain the dynamic power and the static power of a cell?

ii) What are the components in the dynamic power and the static power?

[2.0 Marks]

b) Consider the gate circuit diagram shown in Figure Q5 b) i). The logic waveforms for nodes A, B and E are given in Figure Q5 b) ii).

i) Draw the logic waveforms for nodes C, D and F.

ii) Using the data given for each cell in Page 8 and 9, calculate the followings. (Show all the steps and state any assumption you make)

<u>Hint</u>:
Consider 0 ns – 40 ns window for the calculations. Neglect any transitions at 40 ns.

I) Leakage power, Internal power, Switching power and Total power of U38 in nW (Slew rate for U38 is 0.5 ps and load capacitance is 20 fF)

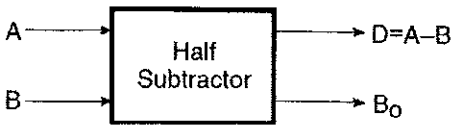
II) Leakage power, Internal power, Switching power and Total power of U39 in nW. (Slew rate for U39 is 0.5 ps and load capacitance is 20 fF)

III) Leakage power, Internal power, Switching power and Total power of U40 in nW. (Slew rate for U40 is 1 ps and load capacitance is 30 fF)

IV) Total power of the design in nW.

[8.0 Marks]

A	B	D	B_O
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



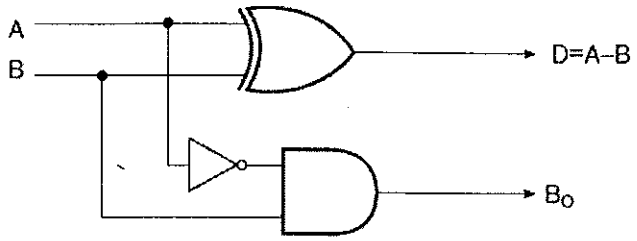


Figure Q1 a) i)

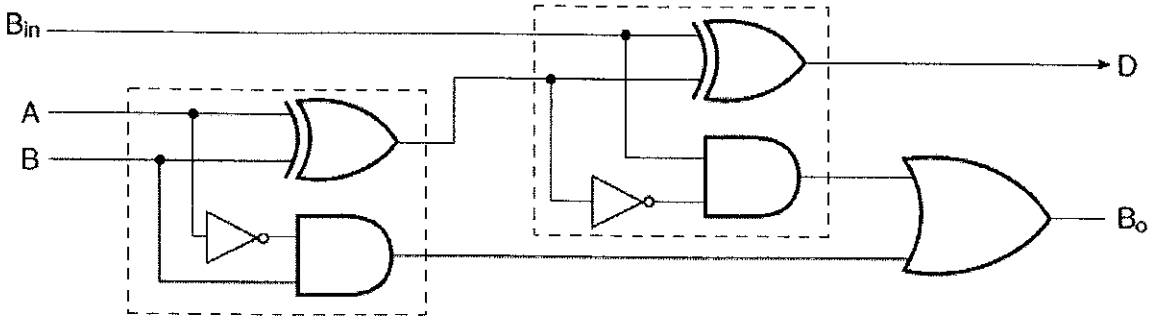


Figure Q1 a) ii)

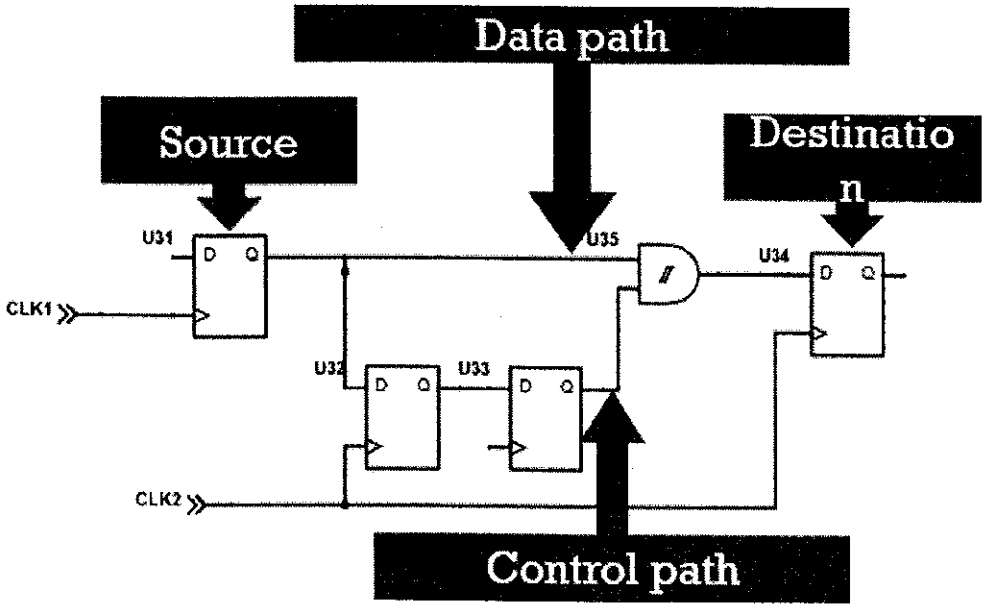
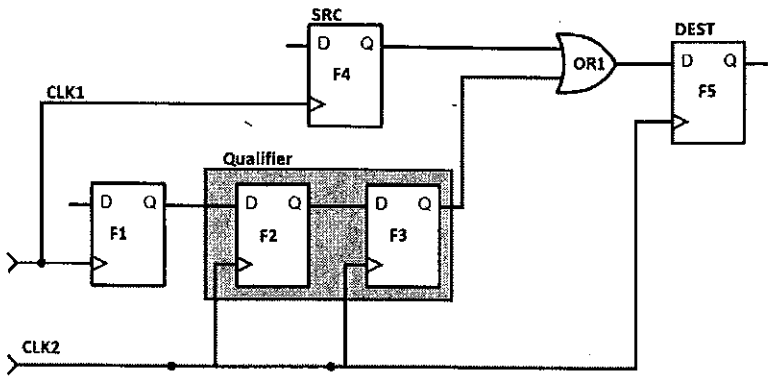
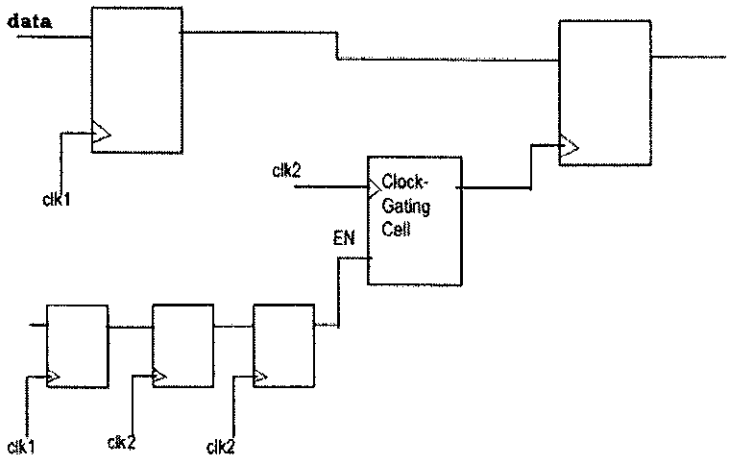
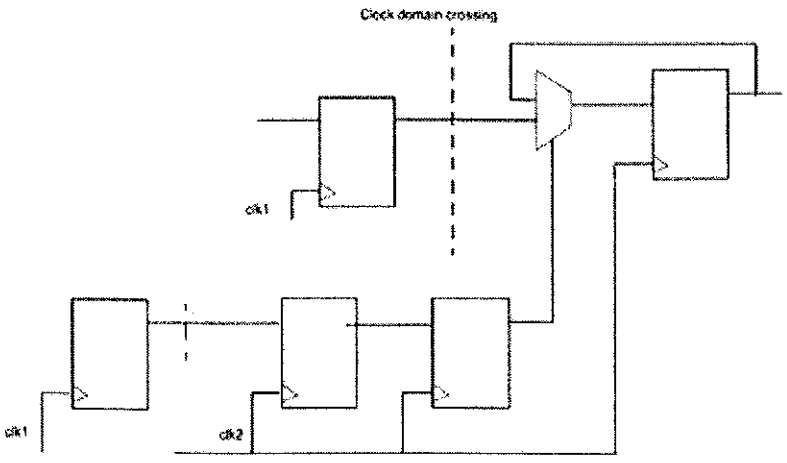


Figure Q3 c)

Table Q3 b)

#	Schematic Diagram	Valid Qualifier (Yes/No)	Blocking Value (0/1/N.A.)
a)			
b)			
c)			

```
    }
    cell (ISOLO) {
        pg_pin(VDD) {
            voltage_name : VDD;
            pg_type : primary_power;
        }
        pg_pin(VDDAON) {
            voltage_name : VDD;
            pg_type : backup_power;
        }
        pg_pin(VSS) {
            voltage_name : VSS;
            pg_type : primary_ground;
        }
        cell_leakage_power : 0.158 ;
        area : 2.52 ;
        cell_footprint : "isolod1"
        is_isolation_cell : true;
        pin(I)  {
            isolation_cell_data_pin : true;
            related_power_pin : VDD;
            related_ground_pin : VSS;
            direction : input;
            capacitance : 0.001145;
        }
        pin(ISO)  {
            related_power_pin : VDDAON;
            related_ground_pin : VSS;
            direction : input;
            capacitance : 0.000771;
            isolation_cell_enable_pin : true;
```

Figure Q4 a) iii (1)

```
 1 create_power_domain top_pd
 2
 3 create_supply_port top_vdd
 4 create_supply_port top_vss
 5 create_supply_port core1_vdd
 6 create_supply_port core2_vdd
 7 create_supply_port core1_vss
 8
 9 create_supply_net top_vdd
10 create_supply_net top_vss
11 create_supply_net core1_vdd
12 create_supply_net core2_vdd
13 create_supply_net core1_vss
14
15 connect_supply_net top_vdd -ports top_vdd
16 connect_supply_net top_vss -ports top_vss
17 connect_supply_net core1_vdd -ports core1_vdd
18 connect_supply_net core2_vdd -ports core2_vdd
19 connect_supply_net core1_vss -ports core1_vss
20
21 set_domain_supply_net top_pd -primary_power_net top_vdd -primary_ground_net top_vss
22
```

Figure Q4 a) iii (2)

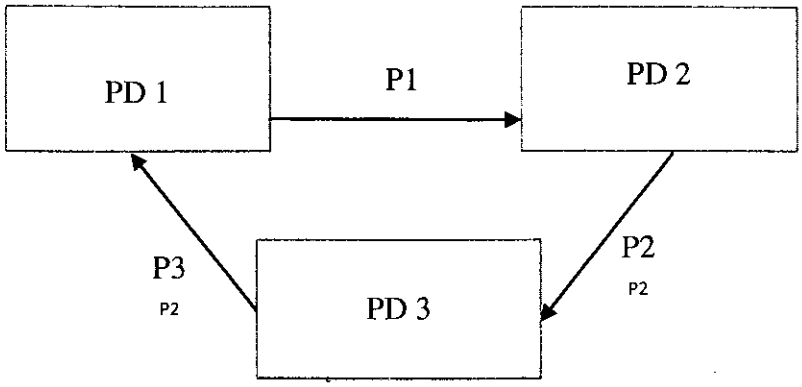


Figure Q4 b)

Table Q4 b)

State	PD1	PD2	PD3
S1	ON (1.1 V)	ON (1.5 V)	ON (1.5 V)
S2	ON (1.1 V)	OFF	OFF
S3	OFF	OFF	OFF

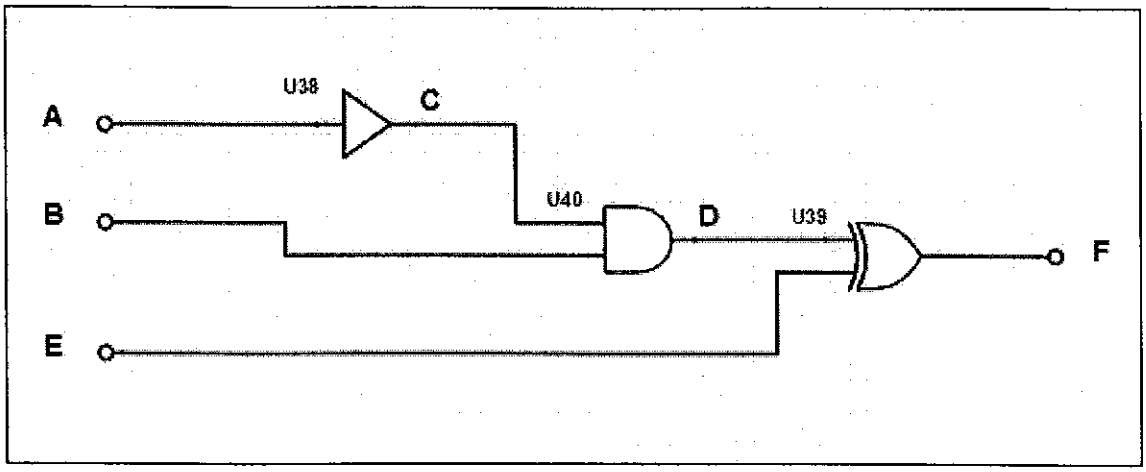


Figure Q5 b) i)

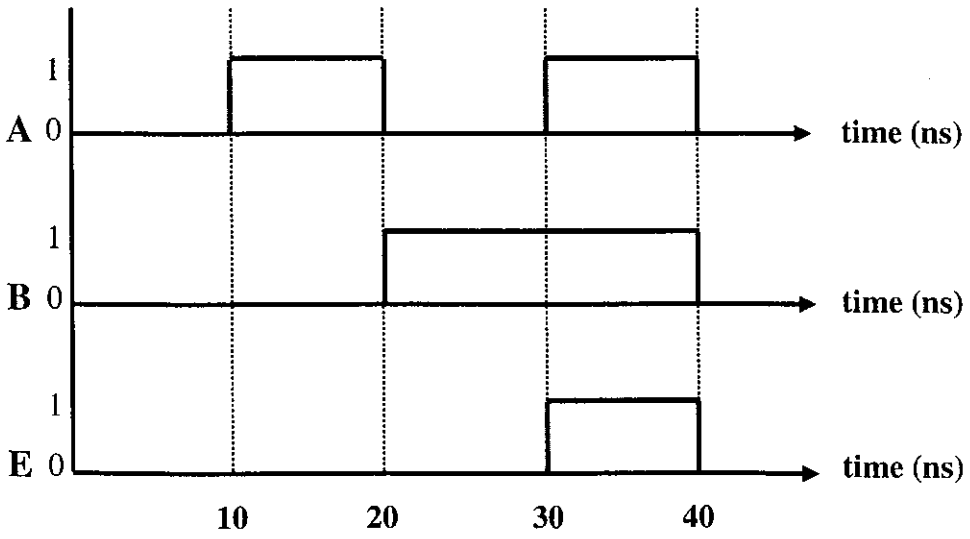


Figure Q5 b) ii)

Common Data for Q5 b)

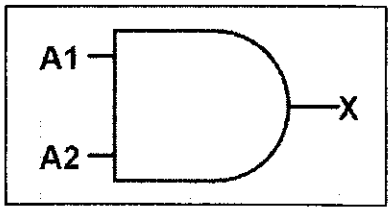
```
/* Units Attributes */
time_unit                       : "1ns";
leakage_power_unit              : "1pW";
voltage_unit                    : "1V";
current_unit                    : "1uA";
energy_unit                     : "1pJ";
pulling_resistance_unit         : "1kohm";
capacitive_load_unit              (1,pf);

/* Operation Conditions */
nom_process                     : 1.00;
nom_temperature                 : 25.00;
nom_voltage                     : 1.20;
```

Notes:

- For internal power tables, values mentioned are energy numbers
- index 1 is the slew rate
- index 2 is the load capacitance
- Switching power of a cell = $0.5 \times C \times V^2 \times f$ where; C is the load capacitance, V is the voltage and f is the frequency.

Data for U40 in Q5 b)




```
cell (AND2_X1) {

        drive_strength          : 1;
        area                    : 1.064000;

        cell_leakage_power      : 8230.017750;

        leakage_power () {
                when            : "!A1 & !A2";
                value           : 4709.287000;
        }
        leakage_power () {
                when            : "!A1 & A2";
                value           : 11031.990000;
        }
        leakage_power () {
                when            : "A1 & !A2";
                value           : 4896.084000;
        }
        leakage_power () {
                when            : "A1 & A2";
                value           : 12282.710000;
        }
```

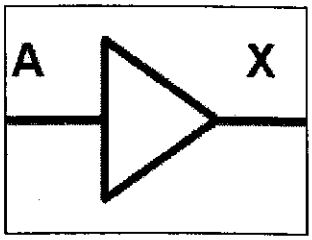
```
pin (X) {

  internal_power ()
  {
        index_1 ("0.0001,0.0005,0.001,0.005,0.01,0.05")
        index_2 ("0.001,0.015,0.020,0.025,0.030,0.035")

        fall_power(Power_data_X1) {
                values ("0.001668,0.001671,0.001674,0.001678,0.001680,0.001681", \
                        "0.001669,0.001672,0.001676,0.001680,0.001682,0.001684", \
                        "0.001722,0.001722,0.001724,0.001728,0.001730,0.001731", \
                        "0.001878,0.001873,0.001870,0.001869,0.001870,0.001870", \
                        "0.003120,0.003085,0.003057,0.003034,0.003018,0.003008", \
                        "0.005017,0.004963,0.004916,0.004867,0.004823,0.004793");
        }
        rise_power(Power_data_X1) {
                values ("0.001196,0.001201,0.001208,0.001219,0.001255,0.001289", \
                        "0.001198,0.001201,0.001207,0.001217,0.001253,0.001289", \
                        "0.001233,0.001234,0.001236,0.001243,0.001277,0.001316", \
                        "0.001732,0.001724,0.001710,0.001702,0.001712,0.001740", \
                        "0.002629,0.002608,0.002586,0.002563,0.002537,0.002560", \
                        "0.004567,0.004516,0.004495,0.004461,0.004376,0.004369");
        }
  }

}
```

Data for U38 in Q5 b)



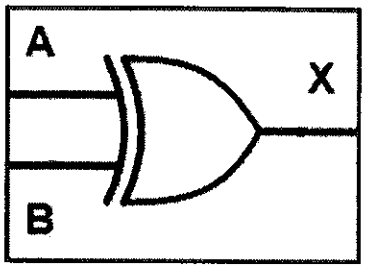

```
  cell_leakage_power      : 2843.729500;

  leakage_power () {
          when            : "!A";
          value           : 1995.972000;
  }
  leakage_power () {
          when            : "A";
          value           : 3691.487000;
  }
```

```
pin (X) {

  internal_power ()
  {
        index_1 ("0.0001,0.0005,0.001,0.005,0.01,0.05")
        index_2 ("0.001,0.015,0.020,0.025,0.030,0.035")
        fall_power(Power_data_X1) {
                values ("0.000140,0.000144,0.000147,0.000150,0.000154,0.000154", \
                        "0.000143,0.000145,0.000147,0.000150,0.000153,0.000154", \
                        "0.000177,0.000170,0.000164,0.000160,0.000157,0.000156", \
                        "0.000302,0.000272,0.000239,0.000211,0.000176,0.000167", \
                        "0.001449,0.001334,0.001160,0.000931,0.000512,0.000380", \
                        "0.003111,0.002969,0.002744,0.002347,0.001319,0.000917");
        }
        rise_power(Power_data_X1) {
                values ("0.000717,0.000723,0.000731,0.000757,0.000778,0.000814", \
                        "0.000733,0.000732,0.000734,0.000753,0.000773,0.000818", \
                        "0.000789,0.000780,0.000770,0.000764,0.000777,0.000810", \
                        "0.001262,0.001218,0.001159,0.001016,0.000947,0.000909", \
                        "0.002025,0.001939,0.001817,0.001507,0.001346,0.001193", \
                        "0.003678,0.003538,0.003334,0.002696,0.002346,0.002006");
        }
  }
}
```

Data for U39 in Q5 b)




```
cell_leakage_power      : 36.163718;

leakage_power () {
        when            : "!A & !B";
        value           : 26.394280;
}
leakage_power () {
        when            : "!A & B";
        value           : 42.963030;
}
leakage_power () {
        when            : "A & !B";
        value           : 23.406273;
}
leakage_power () {
        when            : "A & B";
        value           : 51.891290;
}
```

```
pin(X) {
  internal_power() {
    index_1 ("0.0001,0.0005,0.001,0.005,0.01,0.05");
    index_2 ("0.001,0.015,0.020,0.025,0.030,0.035");
    rise_power(energy_template_7x7) {
      values ("0.008699, 0.008734, 0.008800, 0.008894, 0.008838, 0.008606", \
              "0.008848, 0.008884, 0.008953, 0.009012, 0.008979, 0.008769", \
              "0.008667, 0.008662, 0.008678, 0.008692, 0.008638, 0.008429", \
              "0.008948, 0.008911, 0.008858, 0.008797, 0.008691, 0.008468", \
              "0.009898, 0.009836, 0.009714, 0.009528, 0.009289, 0.008956", \
              "0.016676, 0.016483, 0.016137, 0.015591, 0.014848, 0.013857");
    }
    fall_power(energy_template_7x7) {
      values ("0.000849, 0.001075, 0.001132, 0.001156, 0.001186, 0.001259", \
              "0.000921, 0.001091, 0.000980, 0.001179, 0.001313, 0.001311", \
              "0.001030, 0.000997, 0.000992, 0.001092, 0.001162, 0.001305", \
              "0.001115, 0.001090, 0.001128, 0.001294, 0.001361, 0.001461", \
              "0.001916, 0.001870, 0.001805, 0.001776, 0.001757, 0.001791", \
              "0.008418, 0.008206, 0.007848, 0.007357, 0.006784, 0.006199");
    }
  }
}
```