UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5 Examination in Engineering: October 2019

Module Number: EE5201 **Module Name: Computer Architecture**

[Three Hours]

[Answer **all questions**, each question carries 10 marks]

Q1 a) Describe the fetch cycle and the execute cycle of the Von Neumann Machine.

[2 Marks]

b) What is the difference between branch prediction and data flow analysis.

[2 Marks]

c) List TWO changes done to the design to balance the performance difference between the main memory and the processor.

[2 Marks]

d) List TWO obstacles in increasing the clock speed of the processor.

[1 Mark]

e) Describe THREE key concepts of Von Neumann architecture.

[3 Marks]

Q2 a) Describe how the interrupts can help to improve processing efficiently.

[2 Marks]

b) Describe how the performance is increased when handling multiple interrupts with priorities.

[2 Marks]

c) Describe how the performance will suffer when large number of devices are connected to the bus interconnection.

[2 Marks]

d) What are the advantages of using point-to-point interconnect than shared buses?

[2 Marks]

e) What is the purpose of PCIe to PCI bridge in the PCIe configuration?

[1 Mark]

f) What is the advantage of using Direct Memory Access?

[1 Mark]

Q3 a) Describe how a memory word is transferred between the CPU and the main memory with the presence of a single cache memory.

[2 Marks]

b) Describe the difference between the Logical cache and the Physical cache.

[2 Marks]

c) Assume in a direct mapping cache system the memory is addressed using 24-bits. A 3-bit word number is used to select one of the 8 words in that cache line. The cache line are indexed using 14-bit line number. Calculate the number of bocks that map into one cache line.

[2 Marks]

d) Compare the advantages and disadvantages of associative mapping cache memory.

[2 Marks]

e) List TWO advantages of multi-level cache.

[1 Mark]

f) What is the main advantage of set-assotiave mapping over associative mapping?

[1 Mark]

Q4 a) Draw a circuit diagram and explain how a flip-flop is used to hold the logic state 1 and 0 in a static RAM.

[2 Marks]

b) Assume 8-bit word 10111001 is stored in semiconductor main memory Use the following equations to calculate the check bits. In the equations D1 is the least significant bit and D8 is the most significant bit. Calculate the syndrome word if D1 is changed from 1 to 0.

$C1 = D1 \oplus D2 \oplus D4 \oplus D5 \oplus D7$
$C2 = D1 \oplus D3 \oplus D4 \oplus D6 \oplus D7$
$C4 = D2 \oplus D3 \oplus D4 \oplus D8$
$C8 = D5 \oplus D6 \oplus D7 \oplus D8$

[2 Marks]

c) Describe the write operation of a magnetic disk write head.

[2 Marks]

d) Represent M=-7 and S=3 in Two's complement using 4 bits. Use the subtraction rule and calculate M - S.

[2 Marks]

e) Use unsigned binary multiplication to multiply two numbers stored in Q=1011 and M=1010 registers. Assume that the accumulator (A) resistor and carry (C) flag are initialized to zero. Show all the steps in your answer.

[2 Marks]

Q5 a) Describe the data flow of the interrupt cycle.

[2 Marks]

b) Describe how control hazards reduces the performance of a instruction pipeline.

[2 Marks]

c) Describe the problem of cache coherence in a multiprocessor system.

[2 Marks]

d) Explain how a thread and a process is used in the instruction-level parallelism with multiprocessors.

[2 Marks]

e) Explain what are the design changes with Cache Coherent Non-uniform Memory Access (CC-NUMA) compared to Uniform Memory Access (UMA) in a Multiprocessor system.

[2 Marks]