UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5 Examination in Engineering: August 2018

Module No: EE5201 Module Name: Computer Architecture

Part I

Instructions for candidates

- Write your index number on top of every page.
- Question paper contains 40 multiple choice questions.
- Each question carries 0.5 marks.
- Answer all questions. Each question has only one answer.
- **For each question, put an X mark on the letter: (a), (b), (c), or (d) which corresponds to the correct answer, by using a black or a blue pen.**
- Time allowed is 1 hour and 15 minutes.

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1. Which statement is true about the involvement of the ALU and the Control Unit(CU)?
   (a) CU is used in fetch cycle and ALU is used in execution cycle.
   (b) CU is used in fetch cycle and both CU and ALU is used in execution cycle.
   (c) CU is used in execution cycle and ALU is used in fetch cycle.
   (d) CU is used in execution cycle and CU is not used in fetch cycle.

2. Which statement is true about the instruction cycle of the Von Neuman Machine?
   (a) The opcode of the next instruction is loaded to the IR and the address is loaded to MAR.
   (b) Control circuitry interprets the opcode and executes the instruction.
   (c) Opcode temporally stores the address of the next instruction.
   (d) Both (a) and (b).

3. Which statement is false about Integrated Circuits used in third generation computers?
   (a) Can have an entire circuit in a tiny piece of silicon.
   (b) Cost of a chip remained unchanged during rapid growth in density.

(c) Interconnections on the Integrated Circuit are much more reliable than soldered connections.

(d) Moores law is stated before the introduction of transistors.

4. When we consider the equation of Amdahl's law, what is the parameter which has the highest effect on the speed up?

   (a) Number of parallel processors.

   (b) Fraction of the parallelizable code.

   (c) Time to execute program on a single processor.

   (d) None of the above.

5. Main three components of a computer are Processor, Memory and I/O. Which statement is true about their interactions?

   (a) Memory component has an interrupt signal as an input.

   (b) I/O component has interrupt signal as output.

   (c) I/O component has address signals as output.

   (d) CPU component has interrupt signals as output.

6. Which statement is true about data flow analysis of processors?

   (a) The processor analyzes which instructions are dependent on each other's results or data.

   (b) Instructions are scheduled to be executed when ready.

   (c) Instructions are scheduled independent of the original program order.

   (d) All of the above statements.

7. How the system architects have address the data transfer speed lag between main memory and the processor?

   (a) Reducing the frequency of memory access by using cache structures.

   (b) Increasing the number of bits that are retrieved at one time by making DRAMs "wider".

   (c) Use higher-speed buses between processors and memory.

   (d) All of the above statements.

8. Which statement is true about "Interrupts" in processors?

   (a) Interrupt the processor and slows down its process.

   (b) Suspends execution of the current program being executed.

   (c) Proceeds to the fetch cycle and fetches the first instruction in the interrupt handler program.

   (d) Both (b) and (c).

9. Which statement is true about handling multiple interrupts with priorities?

   (a) Interrupt of lower priority to cause a lower priority interrupt to be interrupted.

   (b) Interrupt of lower priority to cause a higher priority interrupt to be interrupted.

   (c) Interrupt of higher priority to cause a lower priority interrupt to be interrupted.

   (d) Interrupts are handled in parallel.

10. What is/are the solution(s) to the problem when connecting large number of devices to the bus interconnection?

    (a) Extent the length of the bus line.

    (b) Allow all the devices to connect at the same time.

    (c) Use multiple bus hierarchies.

    (d) Both (b) and (c).

11. Designers developed multi-core computer chips due to

    (a) The difficulty of dissipating the heat generated on high-density and high-speed chips.

    (b) When thin wires are close together it increases the RC delay.

    (c) The speed which data can be transferred between main memory and the processor has lagged.

    (d) All of the above statements.

12. Which statement is true about the indirect cycle?

    (a) Bits available at MAR are transferred to the MBR.

    (b) Control unit requests a memory write.

    (c) Indirect cycle is the opposite of direct cycle.

    (d) Bits available at MBR are transferred to the MAR.

13. Which statement is true about the interrupt cycle?

    (a) The special memory location is loaded into MAR from the control unit.

    (b) PC will be incremented by one.

    (c) Contents of the PC are transferred to the MAR.

    (d) PC will not be changed.

14. Which statement is false about the Sign-Magnitude representation of Integers?

    (a) There are two representations of Zero.

    (b) Numbers are varying from -128 to 128 when using 8 bits.

    (c) If the sign bit is 0, number is positive and if the sign bit is 1, number is negative.

    (d) Addition and subtraction need to consider both signs of the numbers.

15. Which creates an overflow situation when adding numbers in Tow's Complement representation?

    (a) 1010 + 0101

    (b) 010[illegible] + 0101

    (c) 1101 + 1111

    (d) 0010 +1110

16. What is the correct Tow's Compliment range extension for 16-bits of the number 11001010?

    (a) 1111111111001010

    (b) 0000000011001010

    (c) 1000000011001010

    (d) 1100101011001010

17. What are the partial products obtained in Tow's Compliment multiplication of 1111 x 0011?

(a) 11011101 and 11111010

(b) 11111111 and 11111110

(c) 11111111 and 10101010

(d) 00001111 and 00011110

18. When normalizing a floating point number in binary, it could lead to

(a) Exponent underflow and overflow.

(b) Significand underflow and overflow.

(c) Exponent underflow or overflow.

(d) Significand underflow and Exponent underflow.

19. Which statement is false about Magnetic Disk?

(a) Magnetoresistive (MR) sensor changes the resistance in the presence of magnetic field.

(b) Write head changes the direction of the current when writing.

(c) The data is organized as tracks and sectors.

(d) Disk is a circular platter constructed of magnetic material, called the substrate.

20. Which statement is false about the syndrome word in error correction?

(a) Each bit of the syndrome is 0 or 1.

(b) Detects only the errors in data bits and not in check bits.

(c) For 8 data bits it requires at least 4 check bits.

(d) Syndrome word can be used to correct errors.

21. If Q (1010) and M(1001) multiplied using unsigned binary multiplication, what are the values available at registers A and Q after three cycles?

(a) A is 1001 and Q is 0101

(b) A is 0100 and Q is 1010

(c) A is 0000 and Q is 0101

(d) A is 0010 and Q is 0101

22. What type of parallel processor system is not commercially implemented?

(a) MIMD

(b) MISD

(c) SISD

(d) SIMD

23. Which statement is false about Symmetric Multiprocessors?

(a) Processors can perform the same functions.

(b) Processors share the same main memory and I/O facilities.

(c) Interaction between processors are done by the Operating System.

(d) It can support only two processors.

24. Which statement is true about Multithreading?

(a) One process can have many threads.

(b) Threads acquire the resources.

(c) Process directly involved with the CPU than threads.

(d) Switching process is less time consuming than threads.

25. What are the starting addresses of blocks map into the cache line number 3 under direct mapping with 8-bit tag and 2-bit word?

    (a) 00000C, 01000C, 02000C

    (b) 0C0000, 0C0001, 0C0002

    (c) 000003, 010004, 020005

    (d) 000003, 000004, 000005

26. Which statement is TRUE about Pipelining?

    (a) The computer is decoding the next instruction while one instruction is executed.

    (b) Executing two instructions at the same time.

    (c) The processor looks ahead in the instruction code fetched from memory and predicts which instructions are likely to be processed next.

    (d) All of the above statements.

27. The method of mapping the consecutive memory blocks to consecutive cache blocks is called

    (a) Set-Associative.

    (b) Associative.

    (c) Direct.

    (d) Indirect.

28. MAR is a register in Von Neumann Machine. Which statement is true about MAR?

    (a) Contains the address of the next instruction pair to be fetched from memory.

    (b) Specifies the address in memory of the word to be written from or read into the MBR.

    (c) Contains a word to be stored in memory or sent to the I/O unit, or is used to receive a word from memory or from the I/O unit.

    (d) Both (b) and (c).

29. Local bus is one bus type under Multiple-Bus Hierarchies. What two components are interconnected by the local bus?

    (a) Processor and main memory.

    (b) Processor and I/O.

    (c) Processor and cache.

    (d) Main memory and I/O.

30. Which statement(s) is/are true regarding set-associative mapping under cache design?

    (a) Has the strengths of both the direct and associative approaches.

    (b) Each word maps into all the cache lines in a specific set.

    (c) Each word maps into multiple cache lines.

    (d) Both (a) and (b).

31. What is the Tow's Compliment of 00000000?

    (a) 11111111.

    (b) 10000000.

    (c) 100000000.

    (d) 00000000.

32. If 7 (0111) is divided by 2 (0010) using the Tow's Compliment division what are the values available at registers A

and Q after the first shift and subtract operation?

(a) A is 1110 and Q is 0111.
(b) A is 1110 and Q is 1110.
(c) A is 0000 and Q is 1110.
(d) A is 0000 and Q is 0111.

33. Which statement is false about the flash memory cell?

(a) Floating gate is insulated by a thin oxide layer added to the transistor.
(b) When a large voltage applied across the oxide layer it represent binary 1.
(c) When a large voltage applied across the oxide layer and when it is removed it represents binary 0.
(d) When there are no electrons in the floating gate it represent binary 1.

34. Which statement is false about SRAM and DRAM?

(a) Both static and dynamic RAMs are volatile.
(b) SRAM is more dense and less expensive than a corresponding DRAM.
(c) DRAM requires the supporting refresh circuitry.
(d) SRAMs are somewhat faster than DRAM.

35. What is Two's complement of -128 (10000000)?

(a) 00000000
(b) 10000000
(c) 01111111
(d) 00000001

36. Number of cycles require to complete each stage in instruction pipelining?

(a) 6
(b) 5
(c) 1
(d) Can't predict

37. L3 Cache supposed to cache the content of?

(a) L2 Cache
(b) Main memory
(c) L4 Cache
(d) Registers

38. The logical address is converted to physical address using

(a) Program Counter
(b) MAR
(c) MMU
(d) MBR

39. Address of a memory location in main memory is used to

(a) Access content from memory to CPU.
(b) Differentiate instructions from data.
(c) Refresh the memory locations.
(d) None of the above.

40. What is an example of sequential access memory

(a) Hard Disk
(b) Main Memory
(c) Tape drive
(d) None of the above.