UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 6 Examination in Engineering: December 2018

Module Number: EE6208

Module Name: Introduction to Hardware Description Languages

[Three Hours]

[Answer **all questions**, each question carries **10 marks**]

Q1 a) State the "Moore's" law that relates the integrated circuit complexity with time.

[1.0 Mark]

b) State all steps in the Application Specific Integrated Circuit (ASIC) design flow and briefly explain them.

[5.0 Marks]

c) Briefly explain the term "Logical Synthesis" in ASIC design flow.

[1.0 Mark]

d) What are the areas which are used to optimize the ASIC design after the logical synthesis process?

[1.0 Mark]

e) State the definition of "Slack" in static timing analysis. What are the potential issues for a design, if it has a negative value for the slack?

[2.0 Marks]

Q2 a) i) What is a Hardware Description Language (HDL)?

ii) Give four examples of HDLs used in design and verification of digital systems.

iii) What are the basic HDL abstraction levels used in chip designing? Briefly explain each abstraction level.

[5.0 Marks]

b) i) What is the basic building block of Verilog HDL?

ii) What are the two primary data types in Verilog and what do they represent in a real hardware?

iii) Write a Verilog code for a simple 2 to 1 multiplexer.

Hint:
The multiplexer has two inputs (A and B), select pin (S) and output (X) as shown in Figure Q2 b). Use the conditional operator to evaluate the conditions.

[2.0 Marks]

c) i) Write a Verilog code for the 8-bit Arithmetic Logic Unit (ALU) shown in Figure Q2 c). Consider the opcodes and the corresponding operations for the inputs (In A and In B) given in Table Q2 c).

Hint:
For the carry flag and the zero flag, use an 8-bit status register.

ii) Write a testbench for the ALU in part c) i) that covers the basic functionality.

[3.0 Marks]

Q3 a) i) What is a Clock Domain Crossing (CDC) in a synchronous digital circuit?
ii) Metastability is one of the major CDC issues. Explain this.
iii) State one harmful impact that occurs in a design due to the metastability and discuss how to prevent that.

[4.0 Marks]

b) The main function of a synchronizer is to mitigate the effect due to metastability. The most common synchronizer used by designers is two Flip-Flop (2-FF) synchronizer. Mostly the control signals (qualifiers) in a design are synchronized using 2-FF synchronizers.
i) Describe the functionality of a qualifier in CDC synchronizers.
ii) Indicate the valid qualifiers and the blocking values relate to schematic diagrams given in Table Q3 b). Note that, CLK1 and CLK2 are asynchronous clocks for flip-flops.
(Redraw the table in your answer sheet without "Schematic Diagram" column and indicate the responses.)

[4.0 Marks]

c) In Figure Q3 c), F1 and F2 are flip-flops and there is a CDC from F1 to F2. A designer uses a latch (L1) to synchronize the crossing.

Does the latch stop the metastability, given the metastability occurs at F2 resolves within a half of a clock period ($T_{CLK2}/2$) that drives it? Justify your answer.

Hint:
Draw the waveforms for CLK2 at F2 and L1.

[2.0 Marks]

Q4 Power estimation plays a critical role in ASIC design. Knowing the potential power consumption of the design before fabrication is important to make sure whether the end product is feasible and to find any potential bugs in the design. The power of a chip is determined by calculating the dynamic and static power components of the design.

a) i) What is the internal power of a cell?
ii) List the factors that the internal power depends on.
iii) What is the switching power of a cell?
iv) What factors will determine the switching power?

[4.0 Marks]

b) Consider the gate circuit diagram shown in Figure Q4 b) I). The logic waveforms for nodes A and B are given in Figure Q4 b) II).
i) Draw the logic waveforms for nodes C and D.
ii) Using the data given for each cell in Page 7, calculate the followings. (Show all the steps and state any assumption you make)
I) Leakage power, Internal power, Switching power and Total power of U1 in nW (Slew rate for U1 is 10 ps and load capacitance is 25 fF)
II) Leakage power, Internal power, Switching power and Total power of U2 in nW. (Slew rate for U2 is 5 ps and load capacitance is 15 fF)
III) Total power of the design in nW

[6.0 Marks]

Q5 a) i) Explain the phenomenon of crowbar currents using a suitable diagram.
ii) State one advantage and one disadvantage of using low voltages in electronic chips.
iii) What information is presented in a "Power State Table"?

[5.0 Marks]

b) A small power domain architecture is shown in Figure Q5 b) and its power state table is given in Table Q5 b).
i) State whether isolation cells and/or level shifter cells are needed to be inserted in each path.
ii) What are the types of level shifter cells to be inserted in P1 and P2 if required?
iii) Explain the level shifter type "both".
iv) What is "Static Verification"?

[5.0 Marks]

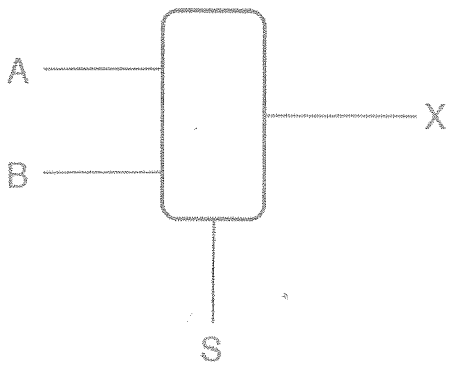


Figure Q2 b)

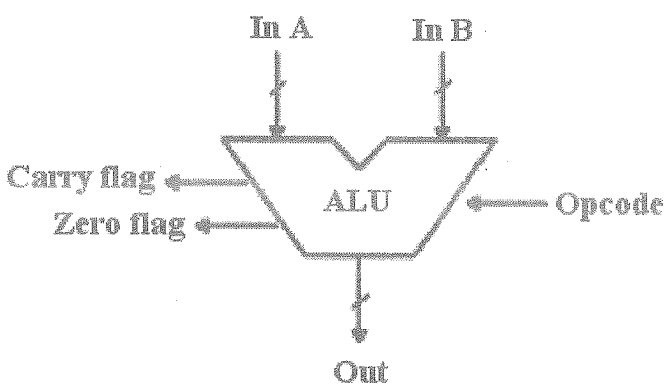
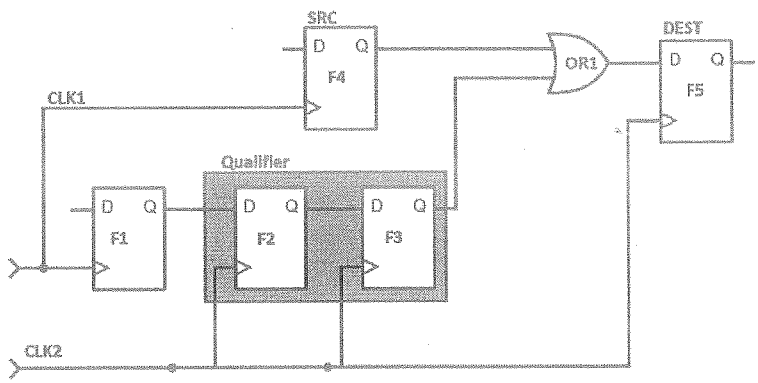
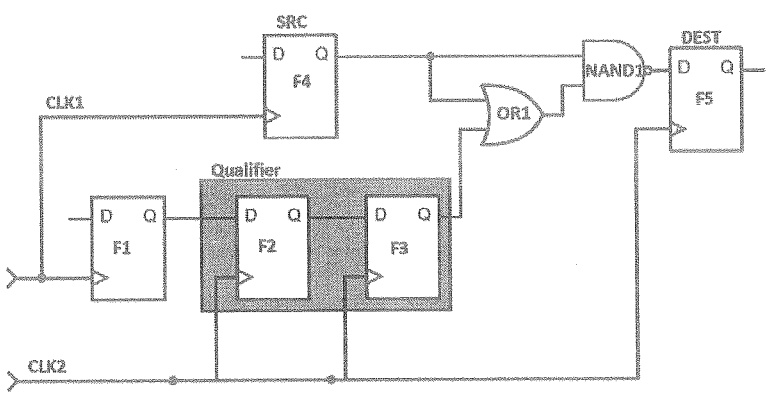
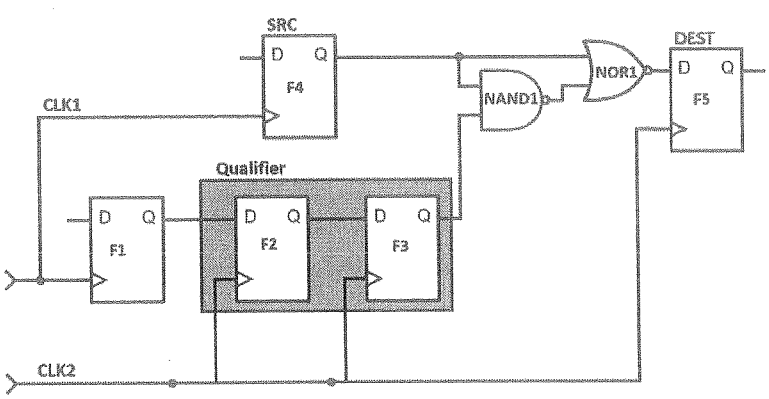


Figure Q2 c)

Table Q2 c)

Opcode	Operation
000	In A
001	In A + In B
010	In A - In B
011	In B - In A
100	In A AND In B
101	In A OR In B
110	In A XOR In B

Table Q3 b)

#	Schematic Diagram	Valid Qualifier (Yes/No)	Blocking Value (0/1/N.A.)
a)			
b)			
c)			

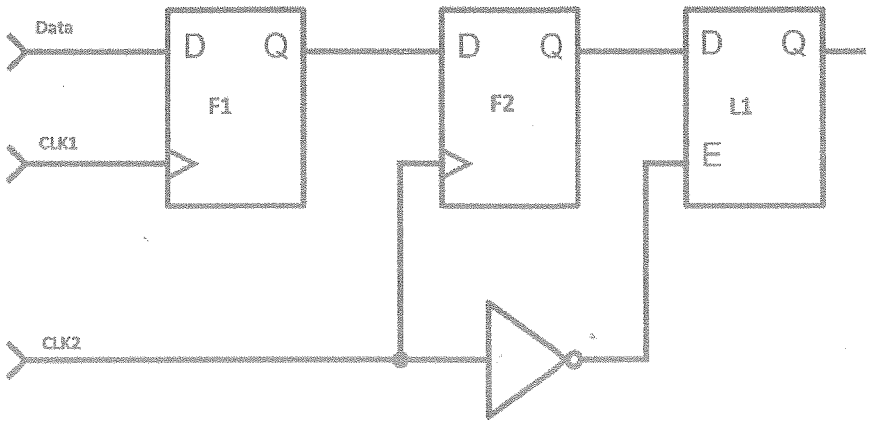


Figure Q3 c)

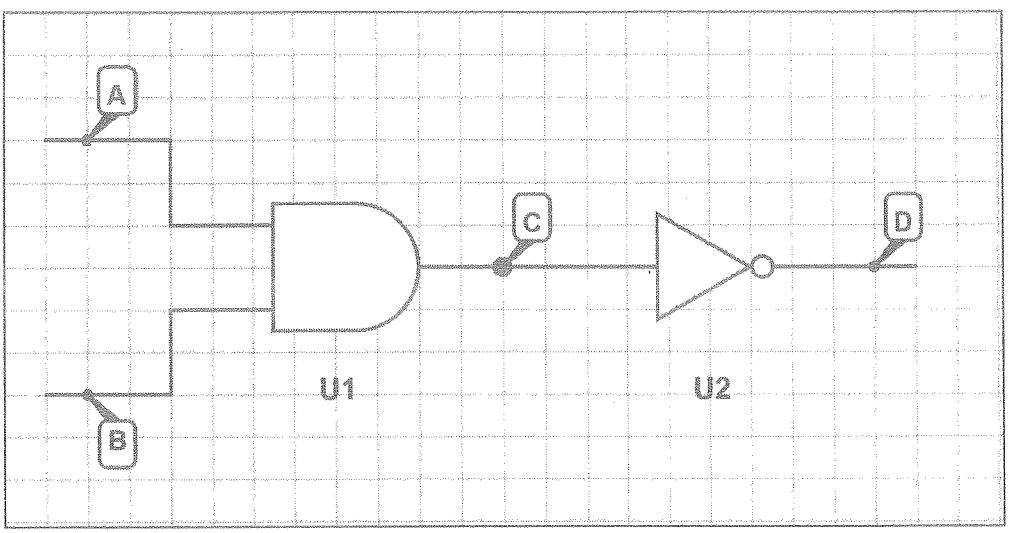


Figure Q4 b) I)

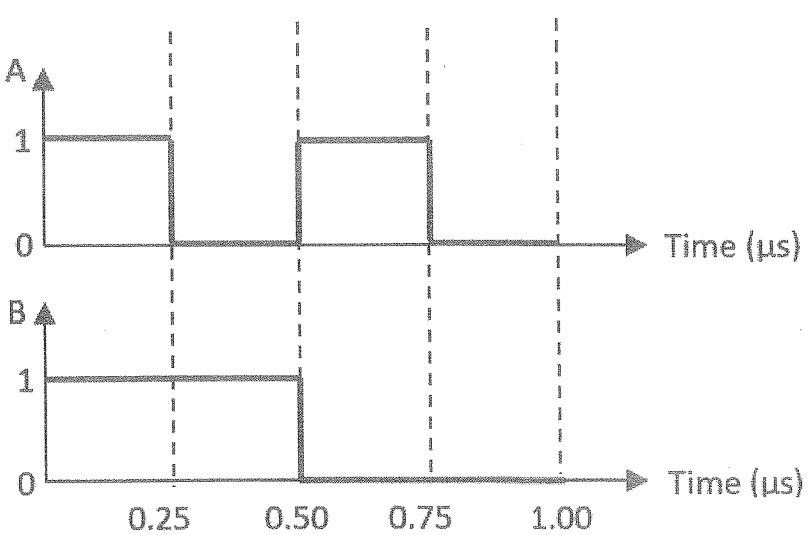


Figure Q4 b) II)

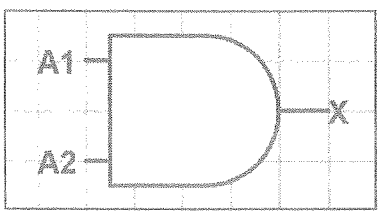
Common Data for Q4 b)

```
/* Units Attributes */
time_unit                       : "1ns";
leakage_power_unit              : "1pW";
voltage_unit                    : "1V";
current_unit                    : "1uA";
energy_unit                     : "1pJ";
pulling_resistance_unit         : "1kohm";
capacitive_load_unit              (1,pf);

/* Operation Conditions */
nom_process                     : 1.00;
nom_temperature                 : 25.00;
nom_voltage                     : 1.20;
```

Notes:

- For internal power tables, values mentioned are energy numbers
- Index 1 is slew rate
- Index 2 is output capacitance
- Switching power of a cell = $C \times V^2 \times f$ where; C is the load capacitance, V is the voltage and f is the frequency.

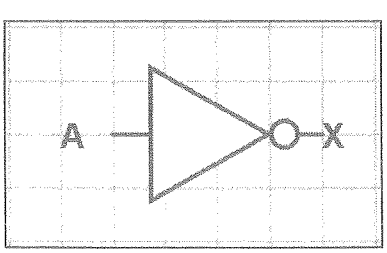
Data For U1 in Q4 b)




```
cell (AND2_X1) {

        drive_strength          : 1;
        area                    : 1.064000;

        cell_leakage_power      : 8230.017750;

        leakage_power () {
                when            : "!A1 & !A2";
                value           : 4709.287000;
        }
        leakage_power () {
                when            : "!A1 & A2";
                value           : 11031.990000;
        }
        leakage_power () {
                when            : "A1 & !A2";
                value           : 4896.084000;
        }
        leakage_power () {
                when            : "A1 & A2";
                value           : 12282.710000;
        }
```

```
pin (X) {

  internal_power ()
  {
        index_1 ("0.0001,0.0005,0.001,0.005,0.01,0.05")
        index_2 ("0.001,0.015,0.020,0.025,0.030,0.035")

        fall_power(Power_data_X1) {
                values ("0.001668,0.001671,0.001674,0.001678,0.001680,0.001681", \
                        "0.001669,0.001672,0.001676,0.001680,0.001682,0.001684", \
                        "0.001722,0.001722,0.001724,0.001728,0.001730,0.001731", \
                        "0.001878,0.001873,0.001870,0.001869,0.001870,0.001870", \
                        "0.003120,0.003085,0.003057,0.003034,0.003018,0.003008", \
                        "0.005017,0.004963,0.004916,0.004867,0.004823,0.004793");
        }
        rise_power(Power_data_X1) {
                values ("0.001196,0.001201,0.001208,0.001219,0.001255,0.001289", \
                        "0.001198,0.001201,0.001207,0.001217,0.001253,0.001289", \
                        "0.001233,0.001234,0.001236,0.001243,0.001277,0.001316", \
                        "0.001732,0.001724,0.001710,0.001702,0.001712,0.001740", \
                        "0.002629,0.002608,0.002586,0.002563,0.002537,0.002560", \
                        "0.004567,0.004516,0.004495,0.004461,0.004376,0.004369");

        }
  }

}
```

Data For U2 in Q4 b)




```
  cell_leakage_power      : 2843.729500;

  leakage_power () {
          when            : "!A";
          value           : 1995.972000;
  }
  leakage_power () {
          when            : "A";
          value           : 3691.487000;
  }
```

```
pin (X) {

  internal_power ()
  {
        index_1 ("0.0001,0.0005,0.001,0.005,0.01,0.05")
        index_2 ("0.001,0.015,0.020,0.025,0.030,0.035")
        fall_power(Power_data_X1) {
                values ("0.000140,0.000144,0.000147,0.000150,0.000154,0.000154", \
                        "0.000143,0.000145,0.000147,0.000150,0.000153,0.000154", \
                        "0.000177,0.000170,0.000164,0.000160,0.000157,0.000156", \
                        "0.000302,0.000272,0.000239,0.000211,0.000176,0.000167", \
                        "0.001449,0.001334,0.001160,0.000931,0.000512,0.000380", \
                        "0.003111,0.002969,0.002744,0.002347,0.001319,0.000917");
        }
        rise_power(Power_data_X1) {
                values ("0.000717,0.000723,0.000731,0.000757,0.000778,0.000814", \
                        "0.000733,0.000732,0.000734,0.000753,0.000773,0.000818", \
                        "0.000789,0.000780,0.000770,0.000764,0.000777,0.000810", \
                        "0.001262,0.001218,0.001159,0.001016,0.000947,0.000909", \
                        "0.002025,0.001939,0.001817,0.001507,0.001346,0.001193", \
                        "0.003678,0.003538,0.003334,0.002696,0.002346,0.002006");

        }
  }
}
```

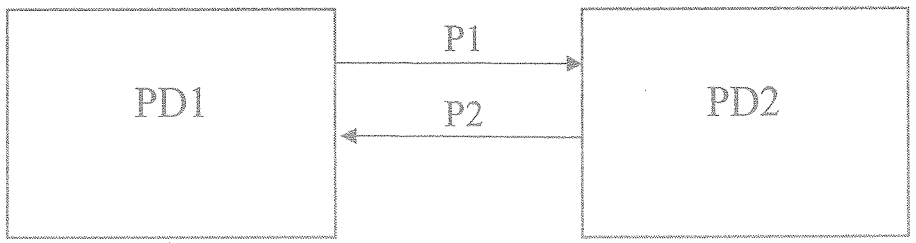


Figure Q5 b)

Table Q5 b)

State	PD1	PD2
S1	ON (1.1 V)	ON (1.2 V)
S2	ON (1.1 V)	OFF
S3	OFF	OFF