UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 2 Examination in Engineering: November 2017

Module Number: EE2202 **Module Name: Introduction to Electronic Engineering**

[Three Hours]

[Answer **all questions**, each question carries **10 marks**]

All notations have the usual meanings

Q1 a) i) Explain how the Silicon (Si) NPN and PNP transistors are made.

ii) Give the circuit symbols for a NPN and a PNP transistor.

iii) Give the circuit for a NPN transistor biased in Common-Base configuration, define the currents and give the equation that relates the currents.

iv) Give the circuit for a PNP transistor biased in Common-Base configuration, define the currents and give the equation that relates the currents.

v) The emitter current in a NPN transistor is 8.6 mA. If 0.82% of the minority carriers injected into the base recombines with holes and the leakage current is 0.1 μA, find

I. the base current

II. the collector current

III. an approximate value for the current gain α.

[5 Marks]

b) Figure Q1 shows a biased Si transistor.

i) State the configuration of the circuit.

ii) Sketch the output characteristics for this configuration and name the different regions.

iii) If current gain $\beta = 100$, find the bias (Q) point of the circuit in Figure Q1.

iv) Give the circuit for an NPN Si transistor as a switch (inverter) and state the regions in the output characteristics in which the switch operates.

[5 Marks]

Q2 a) The transistor in this question is an NPN Si type.

i) Give the Common-Base amplifier circuit (DC and AC) with source v_s for zero source resistance and no load.

Note: Denote the emitter and collector bias resistors as R_E and R_C.

ii) The AC equivalent circuit for the transistor in Common-Base is shown in Figure Q2. Using the AC equivalent circuit in Q2 a) i) show that the voltage gain = R_C/r_e and the current gain = α.

[2 Marks]

b) i) Calculate the input resistance r_{in} for the transistor in Common-Emitter configuration.

ii) By inference, propose a value for the output resistance of the transistor in Common-Emitter configuration.

iii) State why the Common-Emitter configuration is better suited for voltage amplification than the Common-Base configuration.

iv) Give the AC equivalent circuit for the transistor in Common-Emitter configuration.

v) Give the circuit for the Common-Emitter amplifier circuit (DC and AC) with source v_s for zero source resistance and no load.

vi) Calculate the voltage gain and the current gain for this Common-Emitter amplifier.

vii) Give an expression for the overall voltage gain of the amplifier, if there is a source resistance r_s and load R_L.

viii) Taking the load resistance terms only, show that the overall voltage gain is reduced due to the AC load resistance.

[8 Marks]

Q3 a) i) Give the Common-Collector amplifier model and its AC equivalent circuit for zero source resistance and no load.

ii) By calculation, show that voltage gain for the Common-Collector amplifier is ≈ 1.

iii) State why this amplifier is normally known as an Emitter-Follower.

[5 Marks]

b) Reduce the following Boolean expression using the Karnaugh Map

$$F(A,B,C,D) = \sum (0, 1, 2, 3, 5, 7, 8, 10, 11, 12, 13, 15)$$

[2 Marks]

c) A switching network has two control inputs C1, C2 and one data input D. The output Z for each combination of inputs is decided as follows.

If C1 = C2 = 0 and D = 1, the output is Z = 0

If C1 = C2 = 1, the output is Z = 1

If C1 = 1 and C2 = 0, the output is $Z = D$

If C1 = 0 and C2 = 1, the output is $Z = \overline{D}$

i) Derive the truth table for Z.

ii) Implement the switching network only using minimum number of NAND gates.

[3 Marks]

Q4 a) i) Sketch the structure of a biased N-type JFET and show the terminals, the channel and the biasing voltage sources V_{DS} and V_{GS}.

ii) Sketch the formation of the depletion regions for $V_{GS} = 0$ and $V_{DS} \neq 0$. Hence, explain how the pinch-off takes place in an N-type JFET.

[2 Marks]

b) A transfer curve of an N- type JFET for $V_{DS} = 8$ V is illustrated in Figure Q4 (b).

i) Find the pinch-off voltage $|V_P|$ and the saturation current (I_{DSS}) of the N-type JFET.

ii) Sketch the drain characteristics of the N– type JFET for $V_{GS} = -1, -2, \ldots, -V_P$ V.

Hint :

$V_{DS} = V_{GS} - V_P$

$I_D = I_{DSS} (1 - V_{GS}/V_P)^2$

iii) Sketch the transfer characteristics of the N– type JFET for $V_{DS} = 10$ V.

[5 Marks]

c) i) Using necessary sketches, explain how the depletion type MOSFET can be used in the enhancement mode.

ii) Sketch the structure of an N-type enhancement type MOSFET and explain how the channel is formed.

[3 Marks]

Q5 a) i) Define a flip-flop (FF) of a sequential circuit?

ii) What is meant by *state* of a sequential circuit? If there are *m* different states each with *n* bits, how many flip-flops do you need to implement the memory of the sequential circuit?

iii) Draw the logic diagram of a SR-FF constructed using only NAND gates and explain the characteristics of it.

iv) Draw a logic diagram to illustrate how the gated SR-FF is modified to form the JK-FF and write the characteristic table of the JK-FF.

v) Hence, obtain the characteristic tables for the D-FF and the T-FF.

[5 Marks]

b) The output of a special clocked MN flip-flop (FF) to two inputs M and N is illustrated in Figure Q5 (b) 1.

i) Derive the characteristic table of the MN-FF.

ii) For an MN-FF in Master Slave configuration shown in Figure Q5 (b) 2, draw the output waveforms of the Master Flip Flop and the Slave Flip Flop separately for the given clock signal and the inputs. Assume both outputs are 0 prior to the first clock pulse.

Use Figure Q5 (b) 3 for your answer and attach it to your answer script.

Directions : If you have not answered Q5 b)(i) , you may use the JK FF as the MN-FF in Q5 b)(ii). Note that then you can score only half of the marks allocated for Q5 b)(ii).

[5 Marks]

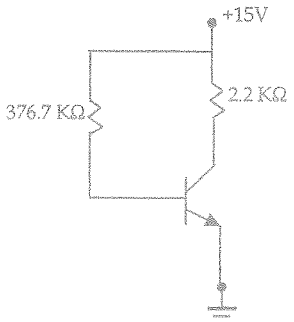

Figure Q1

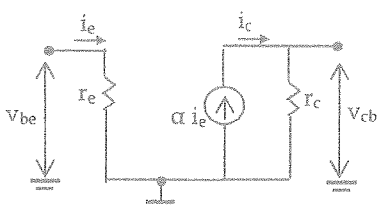

Figure Q2

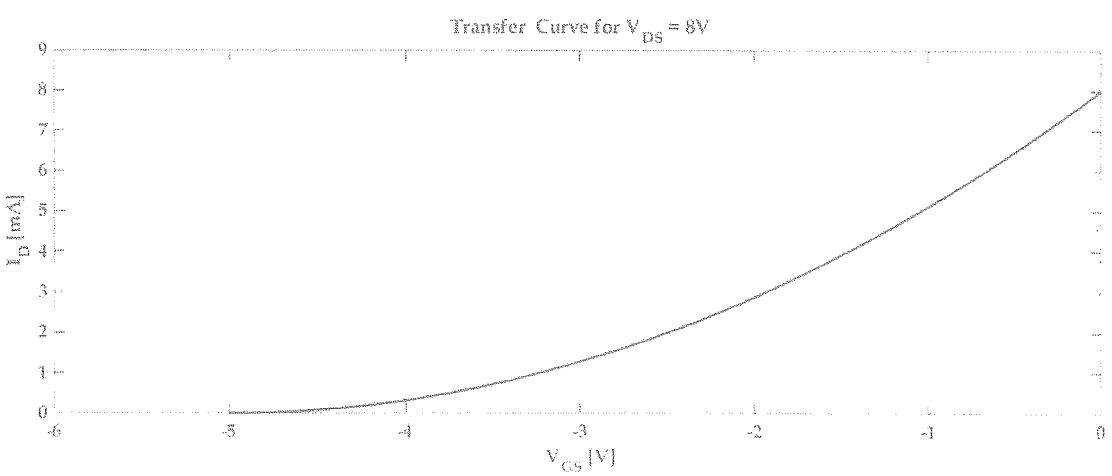

Figure Q4 (b)

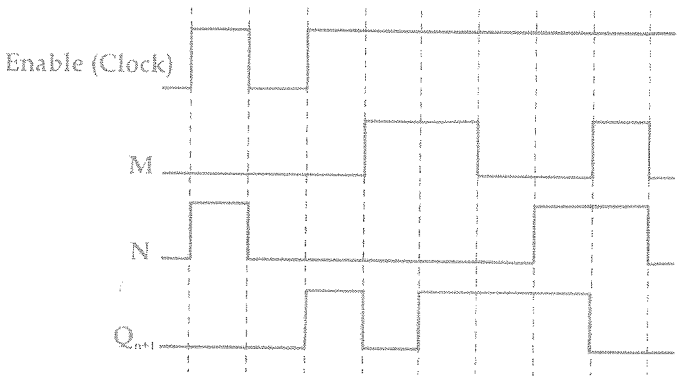

Figure Q5 (b) 1

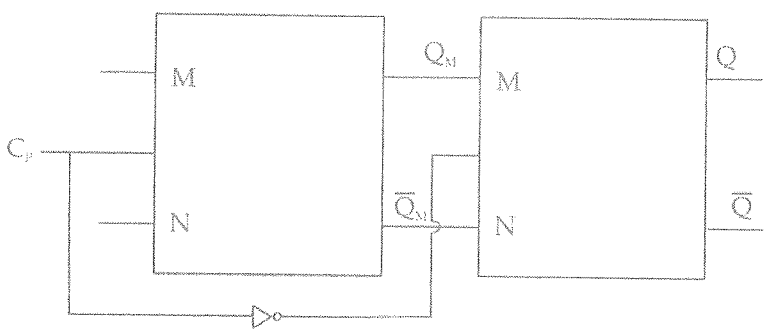

Figure Q5 (b) 2

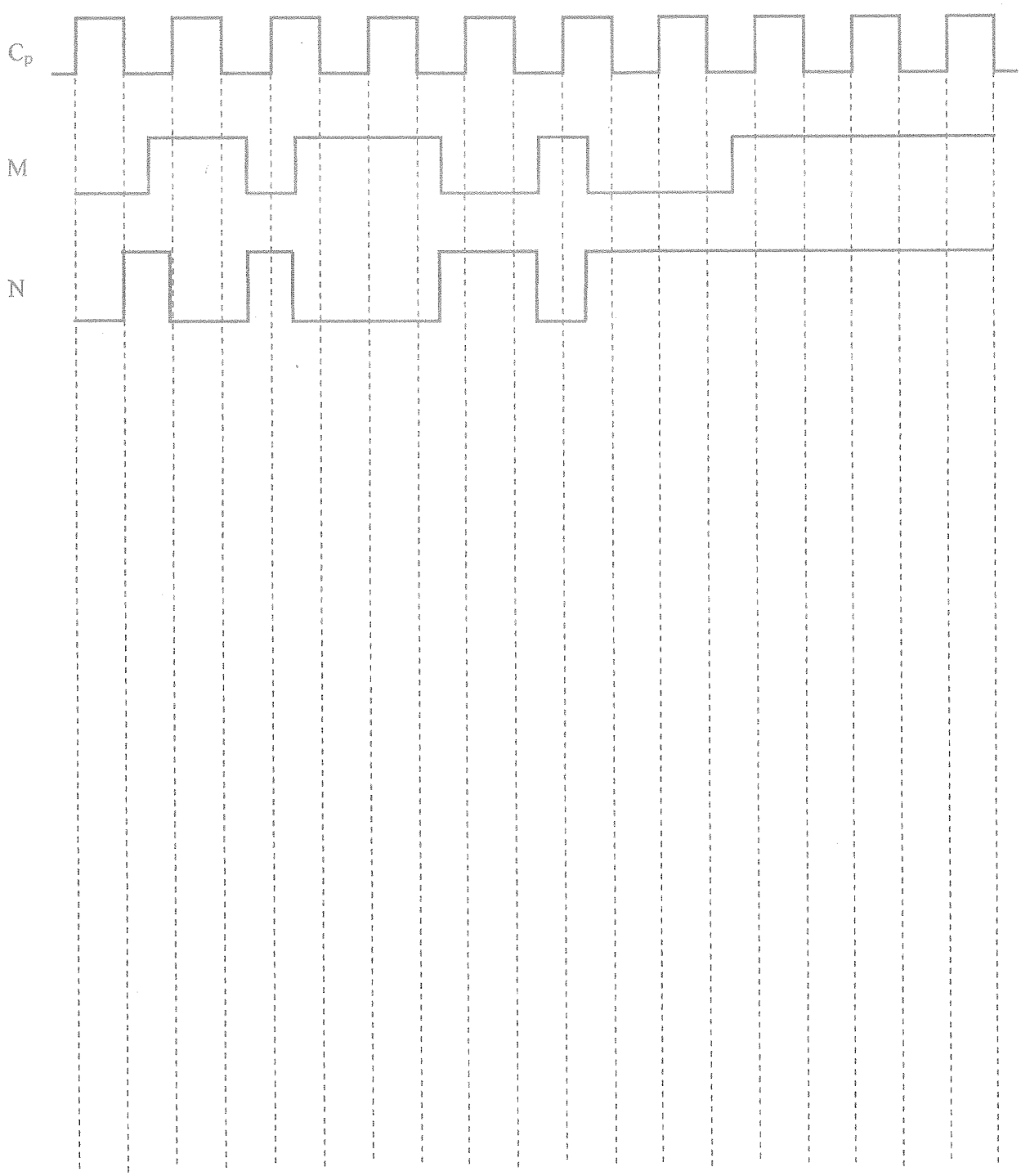

Figure Q5 (b) 3