UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 4 Examination in Engineering: November 2017

Module Number: EE4302 **Module Name: Digital Electronics**

[Three Hours]

[Answer **all questions**, each question carries 12.5 marks]

Note : All the abbreviations have their usual meanings.

Q1 a) i) Briefly explain the synchronism of a synchronous sequential system.

ii) What is meant by triggering of a flip-flop (FF)?

iii) Draw the logic diagram of an edge triggered master-slave D-FF and explain its characteristics.

[3.5 Marks]

b) You are required to analyze the digital circuit given in Figure Q1 (b). In the circuit a special clocked MN flip-flop (FF) is used. The MN FF has two inputs M and N and it operates as follows.

- If MN = 00, the next state of the FF output is 1.
- If MN = 01, the next state of the FF output is the same as present.
- If MN = 10, the next state of the FF output is the complement of present.
- If MN = 11, the next state of the FF output is 0.

i) Derive the characteristic table and the excitation table of the MN FF.

ii) The input functions of the FFs are :

$M_A = (\overline{x + A + B})(\overline{A} + \overline{B})$ - (1) $\quad M_B(x, A, B) = \sum(0,2,3,4,6,7)$ - (3)

$N_A = (\overline{xB} + x)(A + \overline{B})$ - (2) $\quad N_B(x, A, B) = \sum(0,1,4,5)$ - (4)

Obtain the state diagram of the circuit given in Figure Q1 (b), for the given input functions.

[4.5 Marks]

c) You are required to design a digital circuit which detects three or more consecutive 1's in a string of bits coming through an input line.

i) Draw the state diagram of the digital circuit.

ii) Tabulate the state table of the digital circuit and hence, obtain the reduced state table of the design.

iii) Implement the digital circuit using the MN-FF obtained in part b) (i).

Directions : If you have not answered Q1 b) (i), you may use JK FFs in your design. But you should note that then you will score only half of the marks allocated for Q1 c) (iii).

[4.5 Marks]

Q2 a) i) Consider the flow table given in Table Q2(a). For the states : *a=00, b=01, c=11, d=10,* illustrate the state transition when inputs (x_1x_2) change from 00 to 10 using a time diagram. Hence, briefly explain the steady state condition of an asynchronous sequential circuit (ASC).

ii) Briefly explain the closed covering condition related with merging a flow table of an ACS.

[3.5 Marks]

b) Consider the primitive flow table given in Table Q2(b).

i) Find all compatible pairs by means of an implication table.

ii) Find the maximal compatibles by means of a merger diagram.

iii) Find a minimal set of compatibles that covers all the states and is closed.

[4.5 Marks]

c) Consider the flow table given in Table Q2(a) and convert it into transition table by assigning the binary values to the states : *a=00, b=01, c=11, d=10.*

i) Determine all race conditions and whether they are critical or non-critical.

ii) Obtain a binary state assignment to avoid critical races in the flow table.

[4.5 Marks]

Q3 a) Explain the operation of a TTL NAND circuit when both inputs A and B are high (+5 V ≡ logical 1).

[2.0 Marks]

b) i) The NOT gate and the AND gate in Figure Q3(b1) have propagation delays of 5 ns and 10 ns, respectively. Draw a timing diagram for the circuit showing X, Y, and Z. Assume that X is initially 0, Y is initially 1, X becomes 1 for 80 ns, and then X is 0 again for 10 ns.

ii) Figure Q3(b2) shows the voltage and current ranges of a CMOS NAND gate. Calculate the noise margins of the gate.

iii) Find the high state and low state fan-outs of the CMOS NAND gate given in part ii), if the current drawn by each driven gate is 40 µA at the high state and the gate has a sink current of 1.6 mA from each driver gate at the low state.

iv) For a TTL NAND gate, the supply voltage is +5 V. The current drawn by the gate at the high state and the low state are 100 µA and 30 mA, respectively. Calculate the average power dissipation of the gate.

[4.0 Marks]

c) In Figure Q3 c), the TTL NAND gate has the collector supply ($+V_{CC}$) of 5 V and a *5 kΩ* load connected to its output. For all the transistors (T_{1-4}), V_{BE} = 0.7 V and $V_{CE(sat)}$ = 0.2 V. $h_{FE1} = 1$, $h_{FE2} = h_{FE3} = h_{FE4} = 30$. All the diodes are silicon.

i) Find the output voltage

I. When both the inputs are high (+5 V).

II. When both the inputs are low (0 V).

ii) What is the minimum value of the load resistance that can be used, if the high state output voltage is not to be less than 3.5 V?

iii) If the output of the given gate (G_1) is connected with another similar gate (G_2), calculate the current drawn from the driven gate (G_2) at the low state of the gate (G_1). Hence, find the low level fan-out of this gate.

iv) Calculate the low level noise margin of the gate.

[6.5 Marks]

Q4 a) i) Briefly explain the main steps involved in analog to digital (A/D) conversion.

ii) Determine the output voltage of the D/A converter shown in Figure Q4(a) when the input is 110.

[3.0 Marks]

b) A discrete system equation is given by,

$$y[n]-\sum_{k=1}^{N} a_k y[n-k]=\sum_{k=0}^{M} b_k x[n-k]$$

i) Obtain the impulse response in the Z-domain.

ii) What is the condition for infinite impulse response (IIR) system.

iii) Find the finite impulse response (FIR) system equation.

[3.5 Marks]

b) You are required to design a digital logic circuit which compares or adds single bit numbers **A** and **B** depending on a control input. When the control input is asserted high, the circuit should work as the comparator and when it is asserted low, it should work as the adder.

i) Define the required input variables and the output variables for your design. Hence, obtain the truth table according to the design requirement.

ii) If you are given a 3x8 decoder, a 4x16 decoder, five OR gates each with 8 inputs and one XOR gate, design the required digital logic circuit by selecting only the required elements.

iii) You are given four 8x1 Multiplexers, two 4x1 Multiplexers, a bank of NOT gates and three AND gates each with three inputs. By selecting the minimum number of elements, design the logic circuit according to the requirement.

[6.0 Marks]

Table Q2(a) : Flow Table.

y_1y_2 \ x_1x_2	00	01	11	10
a	a, 0	a, 1	b, –	d, –
b	a, –	b, 0	b, 0	c, –
c	a, –	–, –	d, –	c, 0
d	a, –	a, –	d, 1	d, 1

Table Q2(b) : Primitive Flow Table.

x_1x_2	00	01	11	10
a	a, 0	f, –	–, –	e, –
b	c, –	–, –	e, –	b, 0
c	c, 0	d, –	–, –	b, –
d	c, –	d, 0	f, –	–, –
e	a, –	–, –	b, –	e, 1
f	a, –	f, 1	d, –	–, –

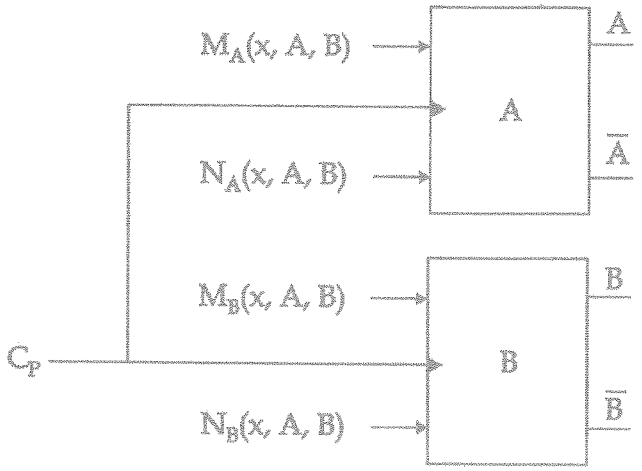

Figure Q1(b)

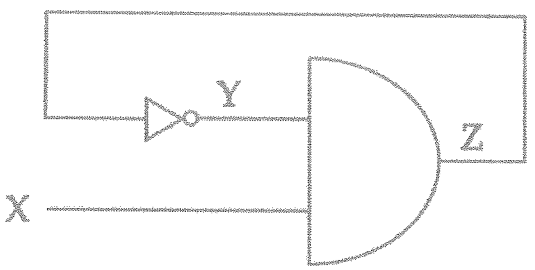

Figure Q3(b1)

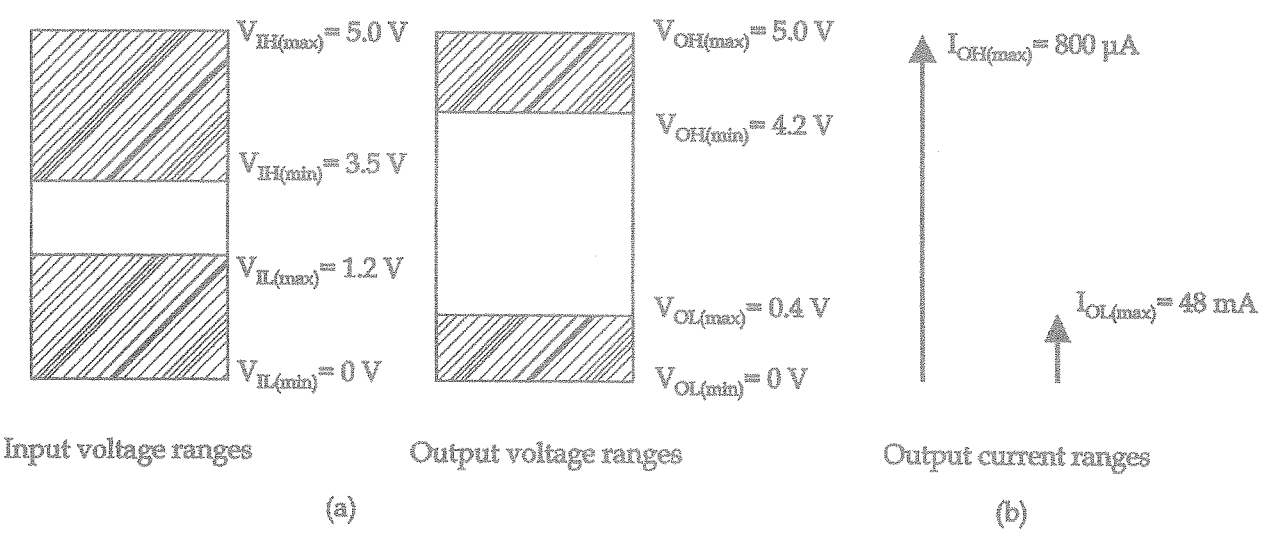

Figure Q3(b2): Voltage and current ranges of a CMOS NAND gate

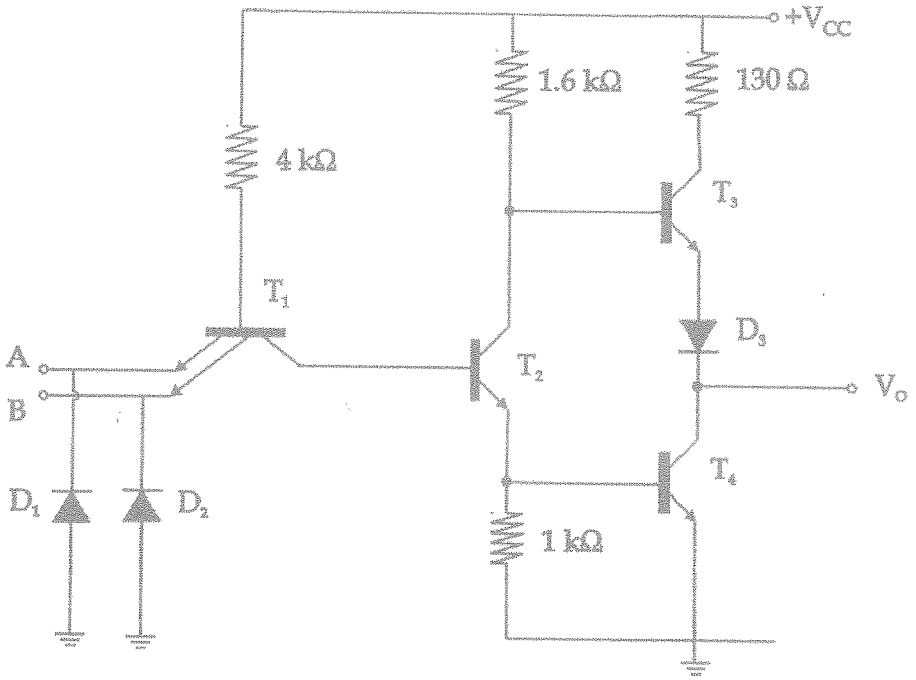

Figure Q3(c): TTL NAND Circuit

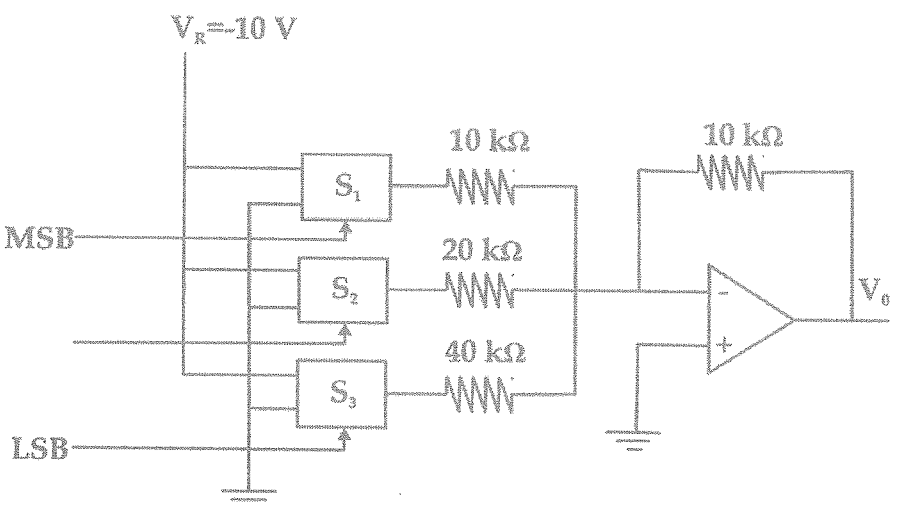

Figure Q4(a): Summing D/A converter Circuit