UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 4 Examination in Engineering: November 2017

Module Number: ME 4311 **Module Name: Analog and Digital Electronics**

[Three Hours]

[Answer **all questions**, each question carries **twelve** marks]

All assumptions must be stated clearly. Sketches and diagrams are to be provided where required. Symbols stated herein denote standard parameters.

Q1 a) Real voltage amplifiers differ from ideal voltage amplifiers. Not only, the input resistance is not infinite and the output resistance is not zero, but the amplifier works properly only in certain conditions. One should always be aware of the range where the circuit acts as a linear (ideal) amplifier, i.e., the output is proportional to the input with the ratio of $A_v = V_o/V_i$ = constant.

i) "Amplifiers do not create power. Rather, they act as a valve adjusting the power flow from the power supply into the load according to the input signal". Briefly explain the voltage supply limit of voltage amplifiers with respect to the above statement.

ii) Derive an expression for the range of the input voltage V_i in which the voltage amplifier can be operated without saturation. (Consider voltage saturation limits as V_{sat}^-, V_{sat}^+)

iii) A voltage amplifier has a limited capability in providing the output current. The maximum output current limits are called "Short Circuit Output Currents" I_{SC}^-, I_{SC}^+. If a fixed load resistance R_L is connected to the amplifier, obtain an expression for the operable output voltage range V_o of the amplifier.

iv) In Operational Amplifiers (OpAmps), a requirement for stability is that the circuit gain should be less than unity at high frequencies. What is the commonly used technique to reduce the gain at high frequencies and avoid instability in practical OpAmps?

v) "A practical amplifier cannot change its output instantaneously if the input changes suddenly". Briefly explain the above statement.

[8.0 Marks]

b) Figure Q1(b) shows a non-inverting OpAmp. OpAmp manufacturers data shows a unity gain bandwidth, $f_U = A f_C = 10^6 kHz$.

i) Design the non-inverting circuit with a gain (A) of 20 dB to drive a 10 $k\Omega$ load.

ii) Calculate the cut-off frequency and the input impedance of the circuit.

[4.0 Marks]

Q2 a) Modern telephone transmission employs Pulse-Code-Modulation (PCM), where the vocal information is converted to digital signals at the transmission and then reconstructed as analog signals at the receiver. Briefly explain the benefits of the use of PCM signals in such applications.

[2.0 Marks]

b) Many systems accept a digital word as an input signal and translate or convert it to an analog voltage or current. Figure Q2 (b) shows such a ladder type Digital-to-Analog Converter (DAC) system.

i) In the DAC system, the third most-significant bit (MSB) N-3 is 1 and all other bits are zero. Find the voltages at the nodes *N-3, N-2, N-1,* and at the output V_0 in terms of V_R and the Resistors.

ii) For an 8-bit DAC with the least-significant bit (LSB) equals to 1 and all other bits equal to 0, find the voltages at all the nodes, 0,1,2,….. and at the output.

[4.0 Marks]

c) Two temperature sensors, one proximity sensor and one sonar sensor are used in an automated conveyer line to detect respective physical parameters. Temperature sensors produce 0 – 5 *V* signals. The proximity sensor produces a digital signal and the sonar sensor produces a 4 - 20 *mA* current signal. Based on the readings of the sensors, a control algorithm is developed and implemented in NI-Labview to send signals to operate two actuators thereby fulfilling the control objectives. The first actuator is operated by sending a current signal and the second actuator is operated by sending a digital signal. NI-USB 6211 is used as the signal processing unit for reading and writing signals. With the help of the terminal signal labels and the pin-out diagram in Figure Q2(c), build a schematic wiring diagram to show hardware and software interfacing of the sensors, actuators, NI-Labview and DAQ board.

Note: You may draw the wiring diagram in Figure Q2(c) itself in page 5 and attach it with the answer script.

[6.0 Marks]

Q3 a) The use of Butterworth polynomials is a common all-pole approximation of the low-pass characteristic. The biquadratic low-pass transfer function can be expressed as, $H(s) = \frac{H_0}{(s^2/\omega_0^2) + (1/Q)(s/\omega_0) + 1}$. Here, the filter transfer function is further reduced to, $H(s) = H_0 / B(s)$, where $B(s)$ is a Butterworth polynomial whose magnitude is given by, $B^2(\omega) = 1 + (\omega/\omega_0)^{2n}$ with n the order of the polynomial and ω_0 the normalized frequency. Obtain the normalized Butterworth polynomial of a low-pass Butterworth filter that is to provide 40 *dB* attenuation at $\omega/\omega_0 = 2$.

Note: The normalized polynomial table for Butterworth filters is provided as Table Q3 (a) in page 6.

[2.0 Marks]

Q3 is continued to Page 3

b) Briefly state occasion(s) in which Butterworth filters are replaced by Chebyshev filters.

[1.0 Mark]

c) The transfer function of a low-pass Chebyshev filter is given by, $H^2(j\omega) = \frac{H_0^2}{1+\varepsilon^2 C_n^2(\omega/\omega_C)}$ where $C_n(\omega/\omega_C)$ are Chebyshev polynomials defined by

$$C_n(\omega/\omega_C) = \cos(n\cos^{-1}\omega/\omega_C) \quad 0 \le \omega/\omega_C \le 1$$
$$= \cosh(n\cosh^{-1}\omega/\omega_C) \quad \omega/\omega_C > 1$$

The parameter ε is related to the passband ripple γ in decibels by $\varepsilon^2 = 10^{\gamma/10} - 1$. Here ω_C stands for the cutoff frequency of the band pass filter. Determine the order of a 1 *dB* ripple Chebyshev filter that gives a 40 *dB* attenuation at $\omega/\omega_C = 2$.

Note: The normalized polynomial table for Chebyshev filters is provided as Table Q3 (c) in page 6.

[2.0 Marks]

d) The Sallen-key circuit in Figure Q3 (d) uses a non-inverting OpAmp stage to provide positive feedback. The transfer function of this circuit can be expressed as, $H(s) = \frac{A_v}{R_1R_2C_1C_2s^2 + s[C_2(R_1+R_2) + R_1C_1(1-A_v)] + 1}$ where $A_v = 1 + R_b/R_a$ is the main gain of the Op-Amp stage. Further, low pass function gives,

$\omega_0 = \frac{1}{\sqrt{R_1R_2C_1C_2}}$, $Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1(1-A_v) + C_2(R_1+R_2)}$. Assuming $R_1 = R_2$, $C_1 = C_2$, design a low-pass filter having no more than 1 *dB* ripple from dc to 1 *kHz* and that gives a minimum of 40 *dB* attenuation at 2 *kHz*.

[7.0 Marks]

Q4 a) Briefly explain the difference between sequential circuits and combinational circuits by considering their electronic properties.

[1.0 Mark]

b) The reduction in the number of flip-flops in a sequential circuit is referred to as the state-reduction. What are the benefits of having a reduced number of states in a sequential circuit?

[1.0 Mark]

c) A sequential circuit has three flip-flops A, B, C; one input *x_in*; and one output *y_out*. The state diagram is shown in Figure Q4 (c). The circuit is to be designed by treating the unused states as don't-care conditions.

i) Identify the unused states from the state diagram.
ii) Obtain the state table for the present states A, B, C, input *x_in* and output *y_out*.
iii) By using D flip-flops, obtain the state equations and output equations.
iv) Draw the logic diagram of the circuit.
v) Analyze the circuit obtained from the design to determine the effect of the unused states.

Note: A summary of Flip-Flop characteristic and excitation tables is given in page 8.

[10.0 Marks]

Q5 a) An n bit binary counter consists of n flip-flops that can count in binary from 0 to 2^n-1. A three-bit binary counter is to be designed using T flip-flops.

i) Draw the state diagram for a three-bit binary counter.

ii) Obtain the state table for the above binary counter.

iii) Simplify the flip-flop input equations of the counter using Karnaugh Maps.

iv) Draw the logic diagram of the final counter.

[4.0 Marks]

b) What are the benefits of using Programmable Logic Controller (PLC) as a digital controller in many industrial applications?

[1.0 Mark]

C) A PLC programme is to be developed to automate a conveyer system in a manufacturing assembly line. The automation engineer has recognized 5 states in which distinct operations are sequentially carried-out in a repeated pattern as given in the state table in Table Q5(c). Respective outputs and time durations of state transitions are further shown. Xinje XC3-24R PLC unit is to be used to implement the programme.

i) Draw the state diagram to represent the automated process.

iii) Develop a PLC programme to achieve fully automated state transitions and outputs with the help of the guidelines provided in Figure Q5(c).

[7.0 Marks]

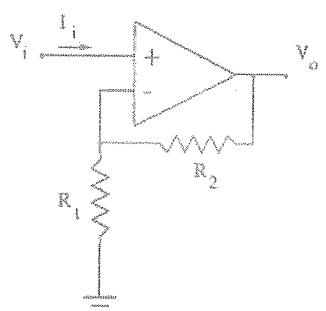


Figure Q1 (b): Non-inverting Amplifier

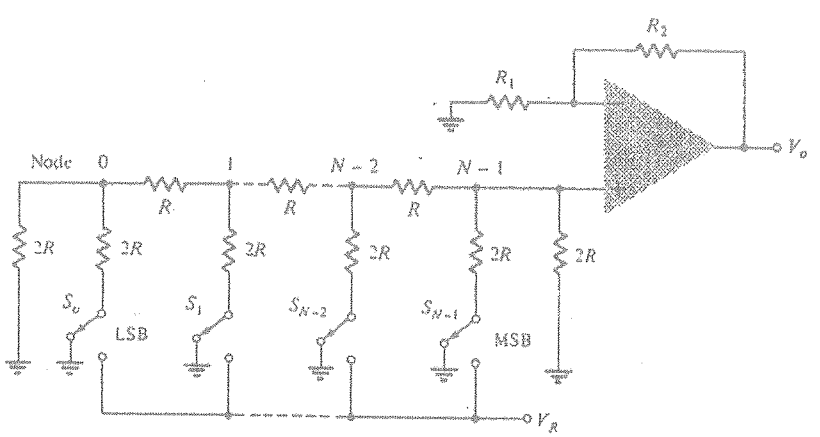


Figure Q2 (b): Ladder Type DAC System

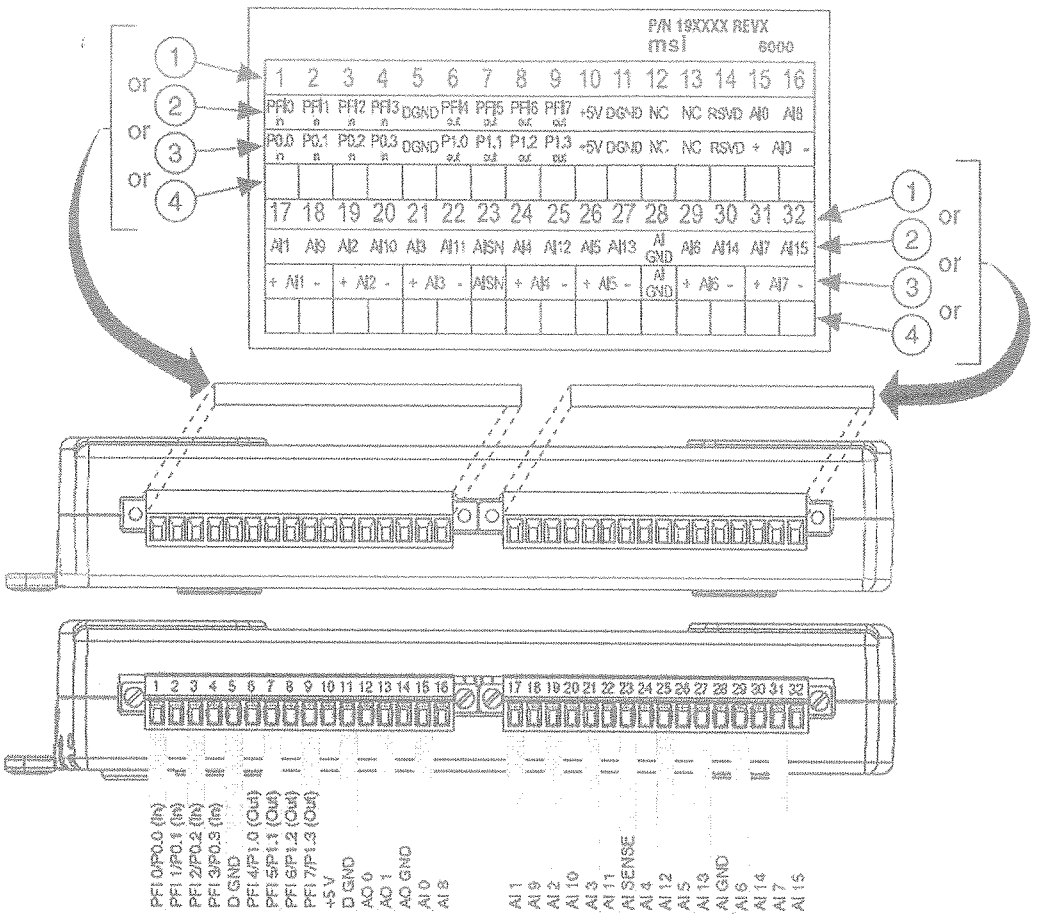


Figure Q2(c): Terminal Signal Labels and Pinout Diagram of NI-USB 6211

Table Q3(a): Normalized Polynomial Table for Butterworth Filters

n	Factors of Polynomial $B_n(s)$
1	$(s+1)$
2	$(s^2+1.4142s+1)$
3	$(s+1)(s^2+s+1)$
4	$(s^2+0.7654s+1)(s^2+1.8478s+1)$
5	$(s+1)(s^2+0.6180s+1)(s^2+1.6180s+1)$
6	$(s^2+0.5176s+1)(s^2+1.4142s+1)(s^2+1.9319s+1)$
7	$(s+1)(s^2+0.4450s+1)(s^2+1.2470s+1)(s^2+1.8019s+1)$
8	$(s^2+0.3902s+1)(s^2+1.1111s+1)(s^2+1.6629s+1)(s^2+1.9616s+1)$

Table Q3(c): Normalized Polynomial Table for Chebyshev Filters

n	Factors of Polynomial $B_n(s)$, *1.0 dB ripple* (ε =0.5089)
1	$s + 1.965$
2	$s^2 + 1.098s + 1.103$
3	$(s + 0.494)(s^2 + 0.494s + 0.994)$
4	$(s^2 + 0.279s + 0.987)(s^2 + 0.674s + 0.279)$
5	$(s + 0.289)(s^2 + 0.179s + 0.988)(s^2 + 0.468s + 0.429)$
6	$(s^2 + 0.1244s + 0.99)(s^2 + 0.3398s + 0.5577)(s^2 + 0.464s + 0.125)$

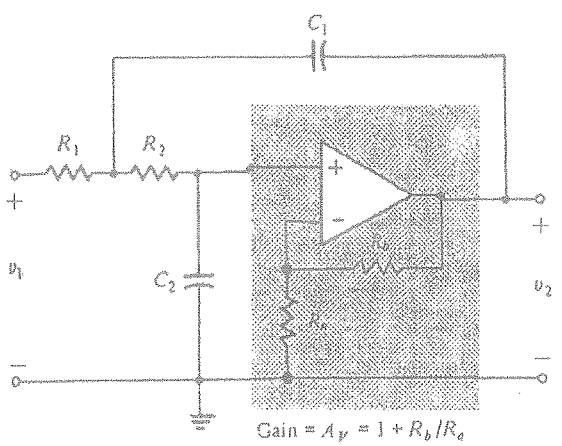


Figure Q3 (d): Sallen-Key Low-pass Sections Using a Noninverting Amplifier

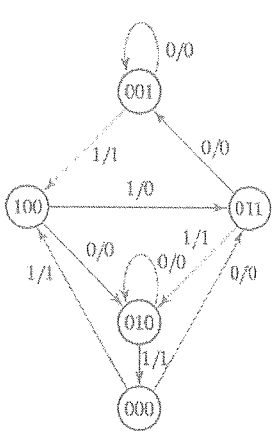


Figure Q4(c): The State Diagram

Table Q5(c): State Table for the Automated Conveyer System

States	Memory States M_0, M_1, M_2	Outputs				Transition Duration (s)
		y_0	y_1	y_2	y_3	
0	000		✓	✓	✓	20
1	001	✓	✓			5
2	010	✓			✓	10
3	011	✓		✓		5
4	100		✓	✓	✓	20

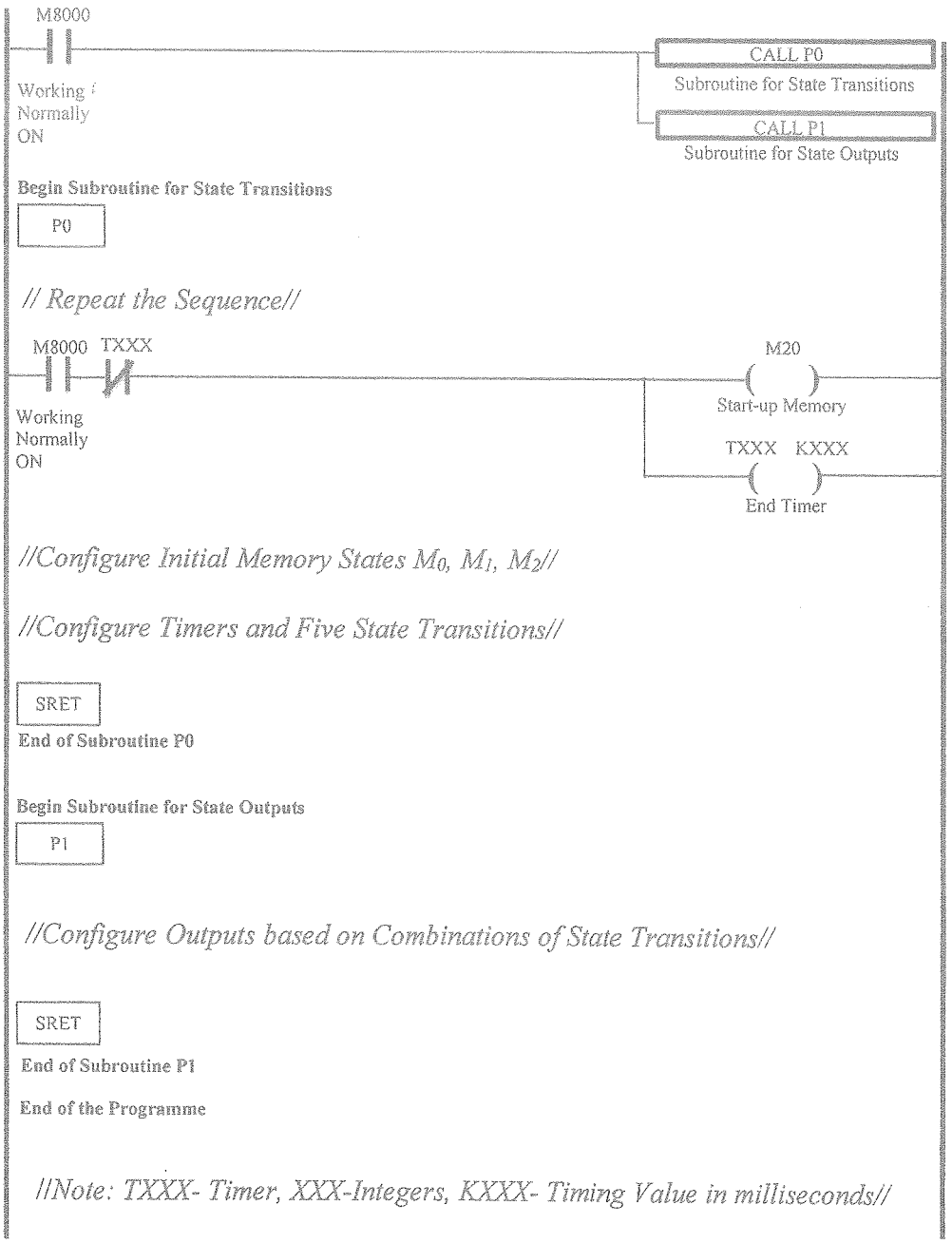
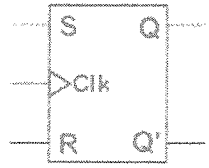


Figure Q5 (c): Guidelines to Develop the PLC Program of the Conveyer System

Summary on Flip-Flop Characteristic and Excitation Tables

SR



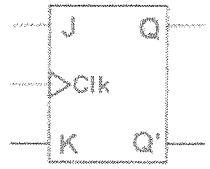
S	R	$Q_{(next)}$
0	0	Q
0	1	0
1	0	1
1	1	?

$Q_{(next)} = S + R'Q$

$SR = 0$

Q	$Q_{(next)}$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

JK

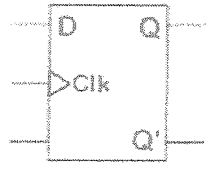


J	K	$Q_{(next)}$
0	0	Q
0	1	0
1	0	1
1	1	Q'

$Q_{(next)} = JQ' + K'Q$

Q	$Q_{(next)}$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D

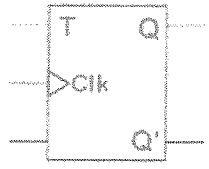


D	$Q_{(next)}$
0	0
1	1

$Q_{(next)} = D$

Q	$Q_{(next)}$	D
0	0	0
0	1	1
1	0	0
1	1	1

T



T	$Q_{(next)}$
0	Q
1	Q'

$Q_{(next)} = TQ' + T'Q$

Q	$Q_{(next)}$	T
0	0	0
0	1	1
1	0	1
1	1	0