UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 6 Examination in Engineering: November 2017

Module Number: EE6208 **Module Name: Introduction to Hardware Description Languages**

[Three Hours]

[Answer **all questions**, each question carries 10 marks]

Q1 a) i) State the "Moore's" law that relates to the integrated circuit complexity over time.

ii) Draw a block diagram for the Application Specific Integrated Circuit (ASIC) design flow and briefly explain each step.

[6 Marks]

b) i) Briefly explain the advantages of Field Programmable Gate Array (FPGA) implementation compared to ASIC implementations.

ii) State the definition of "critical path" in static timing analysis. What are the potential issues, if a design has a negative value for the "critical path"?

[4 Marks]

Q2 a) i) Explain the importance of Hardware Description Languages (HDLs).

ii) What are the uses of HDL languages?

iii) What are the basic HDL abstraction levels? Briefly Explain each abstraction level.

iv) Write a compliable Verilog code for a full adder to show the abstraction levels that are mentioned in part a) iii).

[5 Marks]

b) i) Describe the difference between a latch and a flop using appropriate diagrams.

ii) State the difference between the blocking and non-blocking statements.

[1 Mark]

c) Write the compliable Verilog codes for the following instances.

i) Flop with a synchronous reset and an enable.

ii) Flop with an asynchronous set when the reset = 1, the output = 0, and when the set = 1, the output = 1.

[2 Marks]

d) Create a Verilog test bench for both flops in part c) to simulate their behavior.

[2 Marks]

Q3 a) i) Draw a general architecture of a FPGA and name the structure used to program the FPGA.

ii) For which type of projects and product developments does the FPGAs are more suited compared to the use of ASIC chips?

iii) During the Register Transfer Level (RTL) synthesis step of a FPGA design flow, for what does the following RTL code get synthesized into? (Draw the implementation of the logic output)

```
module addshare (
output oDat,
input iDat1, iDat2, iDat3,
input iSel);
assign oDat = iSel ? iDat1 + iDat2: iDat1 + iDat3;
endmodule
```

[5 Marks]

b) i) Draw the FPGA design flow using a flow diagram.

ii) Explain the RTL Synthesis step of the FPGA design flow and how it is different from the ASIC RTL synthesis.

iii) What are the factors that should be considered for a technology mapping of the FPGA design flow?

[5 Marks]

Q4 a) i) Draw a suitable diagram to explain the "crowbar current" using a Complementary Metal Oxide Semi-conductor (CMOS) not gate.

ii) Write two examples where the condition mentioned in part a) i) may be seen in an ASIC circuit.

iii) The input power pin and the output power pin are the two pins in a power switch. Name two other pins you could observe in a power switch and state why they are required.

[5 Marks]

b) Consider the situation given in Figure Q4 that relates to an ASIC circuit. There are two power domains and two data paths in which the direction of data flow are indicated by the arrows.

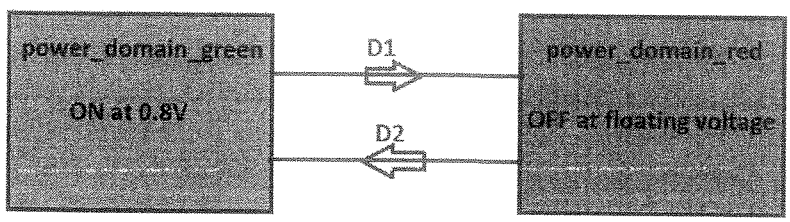

Figure Q4

i) Which protection devices are required for each D1 and D2 data paths?

ii) Consider that the power_domain_red is at 0.6 V. Which protection device is required to be inserted additionally on each D1 and D2 paths?

[3 Marks]

c) i) Write one application of liberty language?

ii) What is meant by the type "both" in a level shifter cell?

iii) Write one reason for zero pin retention cells been more popular among ASIC developers and manufacturers?

[2 Marks]

Q5 Nowadays, designers use multiple clocks having different frequencies in System on Chip (SoC) designs based on multiple reasons. These usages of multiple clocks create multiple clock domains in the design. When the signals transfer through different domains, many issues can happen in the design. These issues are called "CDC issues". Therefore, CDC verification has become one of the major verification challenges in the SoC design flow.

a) i) What is a Clock Domain Crossing (CDC)?

ii) Meta-stability is one of the major CDC issues. Explain why does the meta-stability occur when there is a clock domain crossing?

iii) Mention a harmful impact that occurs in a design due to the meta-stability.

iv) To overcome the meta-stability, designers use different synchronization schemes. Name two such synchronization schemes and draw the diagrams for them.

[5 Marks]

b) Refer the diagram given in Figure Q5 b). There is a clock domain crossing from F1 to F2. F1 and F2 are flip flops. A designer has used a Latch (L1) to synchronize the crossing.

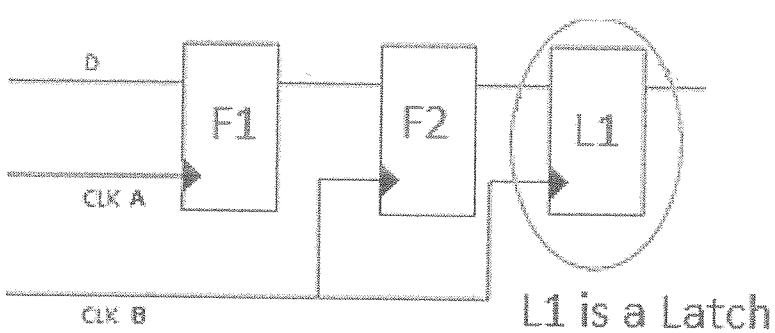

Figure Q5 b)

Can the latch stop the meta-stability? justify your answer.

[3 Marks]

c) A designer came across a structure given in Figure Q5 c) in one of his designs. He concluded that this structure cannot stop the meta-stability and he decided to change the structure. Based on your knowledge, explain why this structure cannot stop the meta-stability.

[2 Marks]

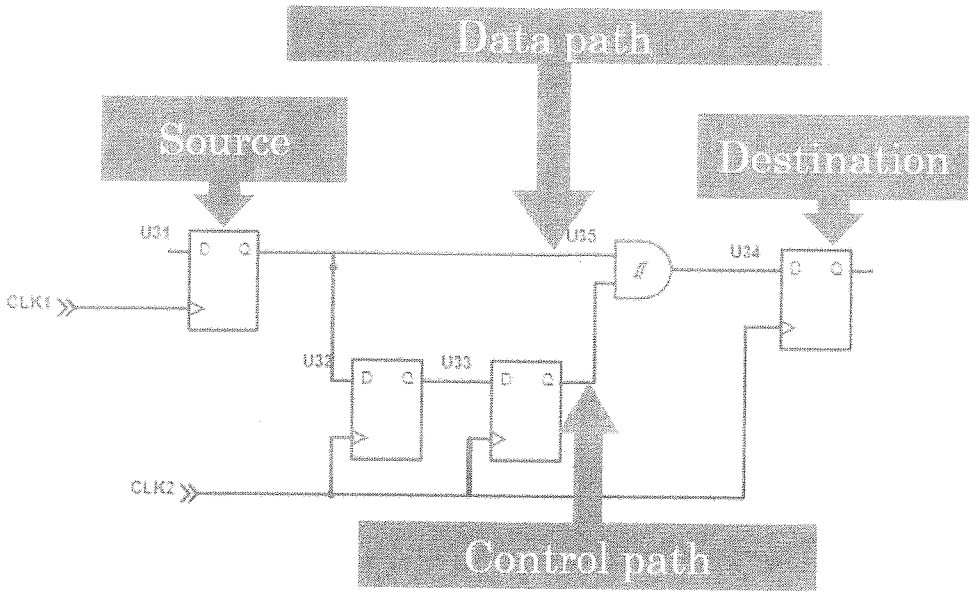
Data path
Source
Destination
U31
U35
U34
CLK1
U32
U33
CLK2
Control path

Figure Q5 c)