UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5 Examination in Engineering: December 2020

Module Number: EE5201 **Module Name: Computer Architecture**

[Three Hours]

[Answer **all questions**, each question carries 12.5 marks]

Q1 a) First generation computers used vacuum tube technology.

i) State two other technologies used by second and third generation computers, respectively.

[1 Mark]

ii) State two input/output technologies used by first generation computers.

[1 Mark]

b) i) State two limitations in increasing the clock speed of microprocessors.

[1 Mark]

ii) State three different bus hierarchies designed to improve the system performance.

[1 Mark]

iii) Compare the single-core architecture with multi-core architecture.

[2 Marks]

c) i) State what is meant by cycles per instruction (CPI).

[1 Mark]

ii) Suppose that a processor executes 25 instructions each taking 5 clock cycles, 65 instructions each taking 4 clock cycles, and 10 instructions each taking 10 clock cycles. calculate the CPI.

[1.5 Marks]

d) i) State two techniques built into the processor to improve the performance.

[1 Mark]

ii) State what is meant by the Speedup of a computer with respect to parallel processing.

[1 Mark]

iii) Suppose that a program with 20% instructions that cannot be executed in parallel is run on a computer with 10 parallel processors. Calculate the speedup that the computer can achieve?

[2 Marks]

Q2 a) Figure Q2.1 shows a block diagram of the Von Neumann architecture. State the functionality of following blocks.

i) PC

ii) IR

iii) MAR

iv) MBR

v) IBR

[0.5 x 5 = 2.5 Marks]

b) Consider the hypothetical machine explained below.

Instruction length: 16 bit

Instruction format: Four most significant bits represent the opcode rest represent operand

List of instructions:

0x00 Load AC from memory

0x01 Store AC to memory

0x02 Add AC from memory

0x04 Add AC to memory

0x08 Clear AC

Snapshot of the machine shown in Figure Q2.2. Machine will start its operation from the given state. Identify the changes to any of the given registers / memory location after executing following.

i) First instruction.

[2 Marks]

ii) Second Instruction.

[2 Marks]

iii) Third instruction.

[2 Marks]

c) i) State three key stages of the instruction cycle.

[1 Mark]

ii) Use a block diagram to explain how an interrupt affects the instruction cycle.

[1 Mark]

iii) Consider an architecture with multiple interrupts. Compare the difference between interrupt service routines when interrupts are with different priorities and all interrupts having the same priority.

[2 Marks]

Q3 a) i) State two performance parameters of memory

[1 Mark]

ii) State the difference between Random access and Sequential access memory, with respect to the access times of different memory locations.

[1 Mark]

iii) State the difference between DRAM and SRAM.

[1 Mark]

iv) State three cache mapping schemes.

[1.5 Marks]

b) i) A processor consists of level 1 (L1) cache with a hit-ratio of 0.9 and access time 0.01 $\mu s$and access time of the main memory is 1 μs. Evaluate average memory access time of this system.

[2 Marks]

ii) Assume that the next version of the processor architecture inserts a level 2 (L2) cache in between L1 cache and the main memory. The hit-ratio of L2 cache is 0.95 and the access time is 0.1 μs. Evaluate average memory access time of the system with L1 cache, L2 cache, and the main memory.
[Hint: Sketch two levels of cache and the main memory and work out the probabilities]

[2 Marks]

c) Assume that an 8-bit data packet is encoded using Hamming codes and stored in the memory. Hamming bits used in encoding are given by

P1 = D3 $\oplus$ D5 $\oplus$ D7 $\oplus$ D9 $\oplus$ D11
P2 = D3 $\oplus$ D6 $\oplus$ D7 $\oplus$ D10 $\oplus$ D11
P4 = D5 $\oplus$ D6 $\oplus$ D7 $\oplus$ D12
P8 = D9 $\oplus$ D10 $\oplus$ D11 $\oplus$ D12

Suppose that the stored data is observed as 100111011111. Assuming that there can be only one-bit errors, identify if there are one-bit errors and the location of the error bit.

[4 Marks]

Q4 a) State the maximum and minimum numbers that can be represented by 10-bit binary numbers when represented using the following methods.

i) Signed magnitude method.

[1 Mark]

ii) Two's complement method.

[1 Mark]

b) Suppose that you have to carry out the binary multiplication 27 x -15 (not -15 x 27) by representing them as 6 bit binary numbers.

i) Evaluate is the two's complement representation of -15

[1 Mark]

ii) Carry out the binary multiplication in the format given in Figure Q4.1

[3 Marks]

c) i) State three pipeline hazards.

[1.5 Marks]

ii) State the type of hazard associated with a wrong prediction of a branch instruction?

[1 Mark]

iii) Explain what a program status word is?

[1 Mark]

d) i) Assuming that each stage of a K-stage instruction pipeline is of duration T, derive an equation for the speedup factor for N instructions.

[2 Marks]

ii) Calculate the maximum speedup that can be achieved due to the pipelining given in above part i)?

[1 Mark]

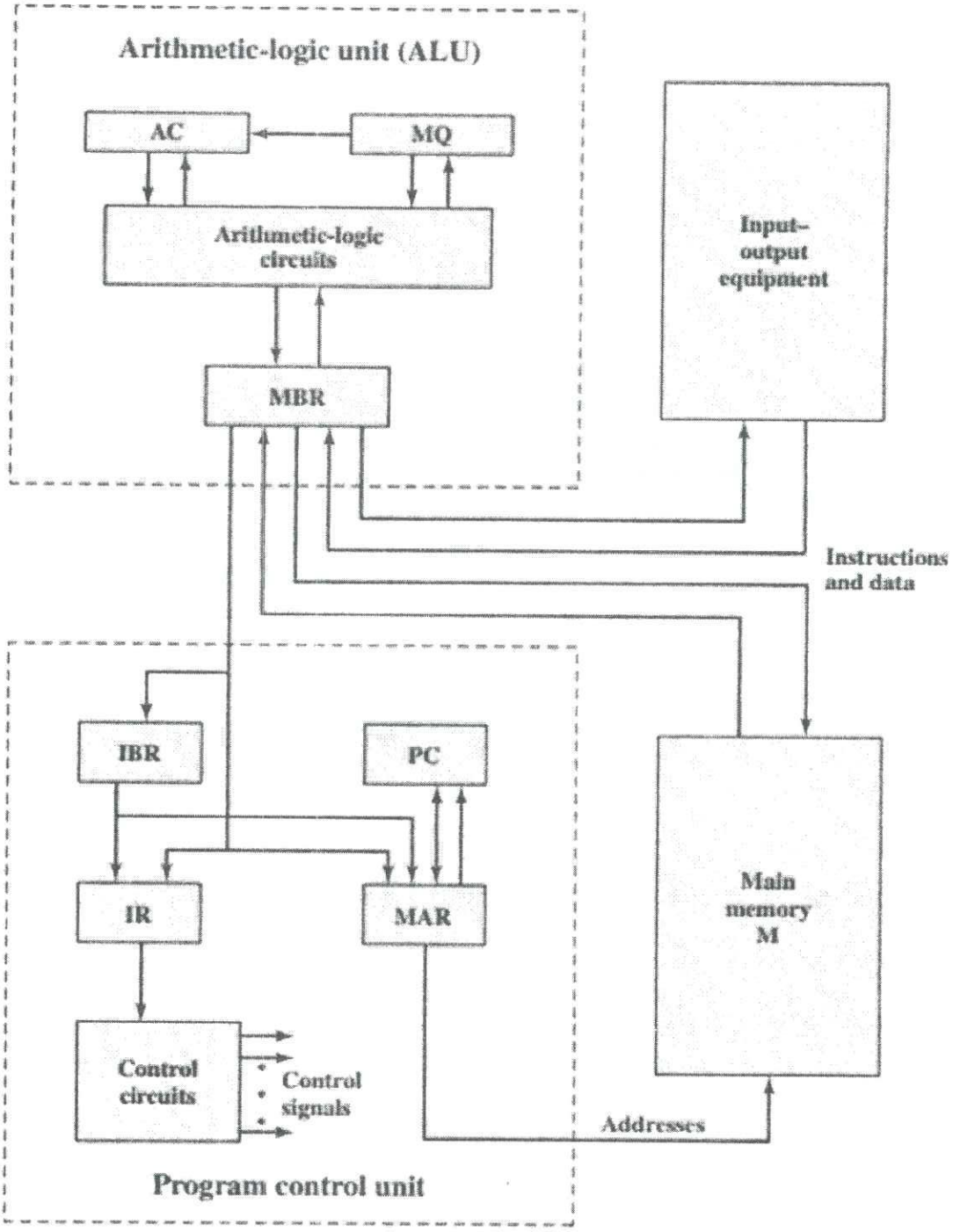
Arithmetic-logic unit (ALU)
AC
MQ
Arithmetic-logic circuits
MBR
Input–output equipment
Instructions and data
IBR
PC
IR
MAR
Main memory M
Control circuits
Control signals
Addresses
Program control unit

Figure Q2.1

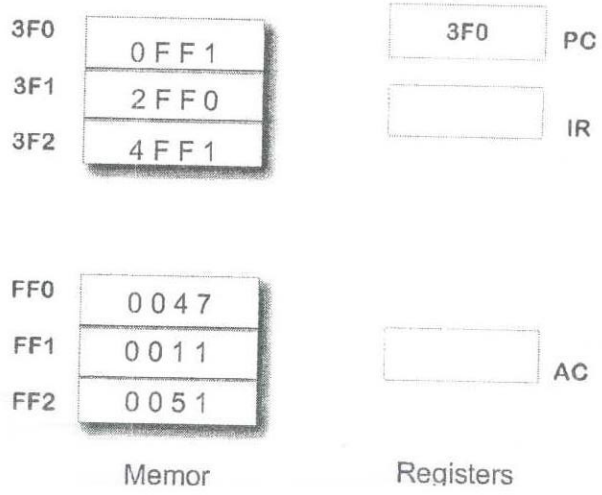

Figure Q2.2

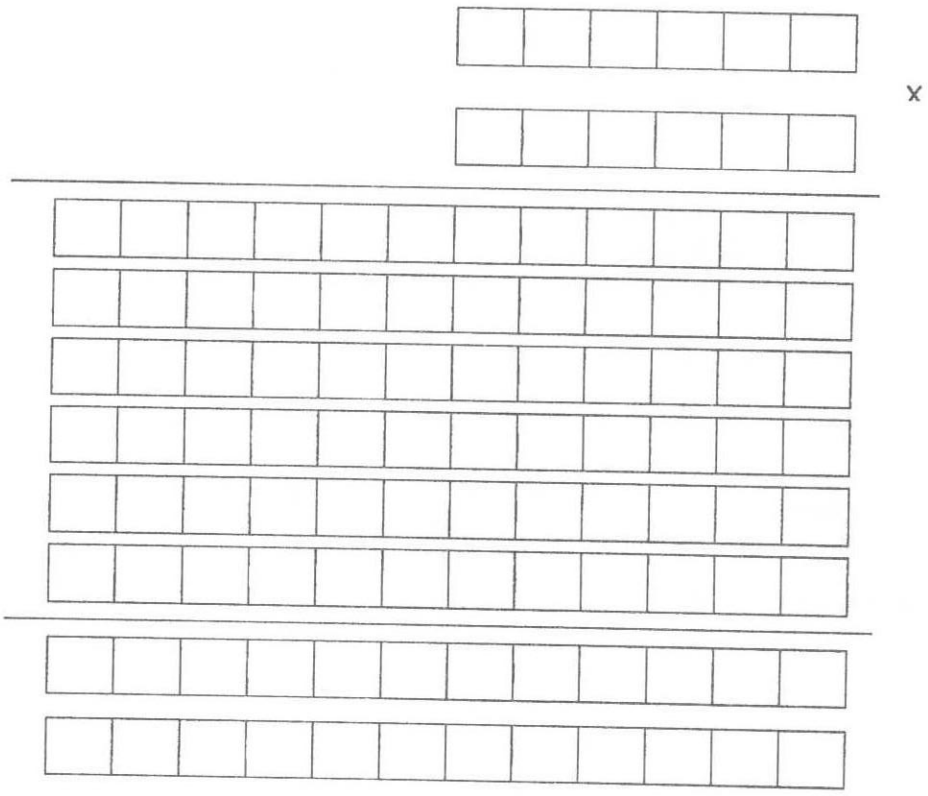

Figure Q4.1