UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 3 Examination in Engineering: July 2016

Module Number: EE3301 **Module Name: Analog Electronics**

[Three Hours]

[Answer **all questions**, each question carries **10 marks**]

All notations have their usual meanings.

Q1 a) Predict that the constant current source I in the circuit in Figure Q1 is mirrored to the collector current of the transistor T2. Assume that T1 and T2 are matched.

[2 Marks]

b) i) Reproduce the circuit of an ideal differential amplifier that has collector bias resistors 6 kΩ, supply voltage +15 V and a constant current source of 2 mA.

ii) Calculate the internal emitter resistance of the transistors for this ideal differential amplifier.

iii) When the input 2 of the ideal differential amplifier circuit is grounded and a sinusoidal signal is applied to the input 1, calculate the magnitude and phase of the voltages at the

I) emitters of the transistors

II) output 1

iv) When the signals ± 20 sin (ωt) mV is applied to inputs 1 and 2 respectively, by inference determine the magnitude and phase of the two output voltages.

[6 Marks]

c) The CMRR is defined as $|A_d| / |A_{cm}|$ where A_d is the output difference voltage caused by common mode signals and A_{cm} the common mode signal respectively.

i) State the meaning of the acronym CMRR.

ii) When the inputs to a differential amplifier are:
$v_{i1} = 0.1 \sin(\omega t)$ and $v_{i2} = -0.1 \sin(\omega t)$
the outputs are: $v_{o1} = -5 \sin(\omega t)$ and $v_{o2} = 5 \sin(\omega t)$

When both inputs are 2 sin (ωt) the outputs are:
$v_{o1} = -0.04 \sin(\omega t)$ and $v_{o2} = 0.04 (\sin \omega t)$

Calculate the CMRR in dB.

[2 Marks]

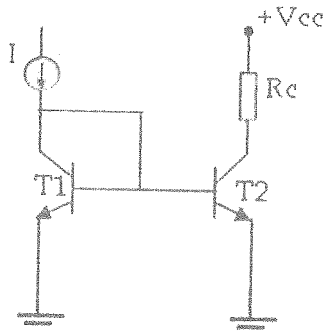

Figure Q1

Q2 a) i) Define the properties of an ideal operational amplifier.

ii) Draw the circuit of an inverting amplifier based on an operational amplifier.

iii) State how the inverting amplifier can be used as a Voltage Follower.

iv) Explain briefly how a Voltage Follower can be used practically.

[2 Marks]

b) For an operational amplifier

i) Sketch the desired frequency response of the open loop gain and denote its characteristic features.

ii) Define the Gain Bandwidth Product (GBP) and the Closed Loop Gain Bandwidth (BW_{CL}) in terms of the GBP.

iii) Define the slew rate.

iv) For a sinusoidal output $V_o(t) = K \sin(\omega t)$, predict the maximum frequency permitted by the slew rate.

[2.5 Marks]

c) For the inverting amplifier in part a), a resistor R_c can be connected in series with the non-inverting input in order to minimize the input offset current.

i) Formulate an expression for the value of R_c.

ii) Show that the output offset voltage due to bias currents are minimized when the input bias currents I_{B^+} and I_{B^-} are equal.

iii) Describe the origin of the input offset voltage and formulate an expression for the output offset voltage due to the input offset voltage.

iv) Express the total output offset voltage for the worst case from the derived expressions.

v) State how the output offset voltage is minmized in practice.

[5.5 Marks]

Q3 a) State the difference between an oscillator and a multivibrator.

[0.5 Marks]

b) Sketch a block diagram of an oscillator and state the necessary conditions for oscillation.

[1 Mark]

c) Figure Q3 c) shows the Colpitts oscillator circuit. $R_1 >> X_{C2}$ where X_{C2} is the reactance of C_2. Determine the oscillating frequency of the circuit and the gain required for the amplifier.

[4 Marks]

d) Explain the difference between a Butterworth and a Chebyshev filter considering their frequency responses.

[1 Mark]

e) Using the data in Table 1 and the circuit in Figure Q3 e), design a second-order low pass Butterworth filter with a cut-off frequency 2.5 kHz and a gain in the passband of 2. The constant $K = 10^{-4}/(fC)$ where f is the desired cut-off frequency in Hz and C is the value of capacitance selected in Farads.

[3.5 Marks]

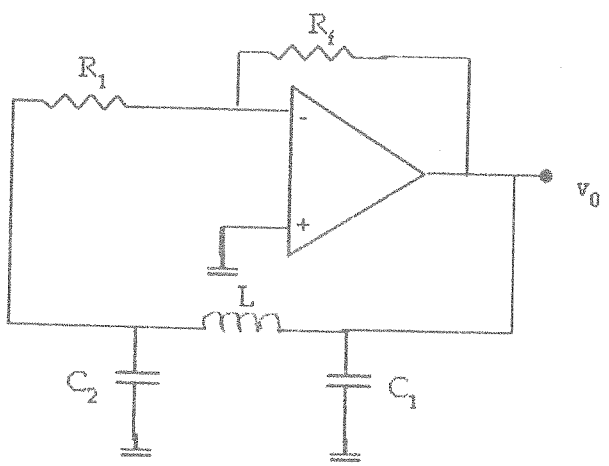

Figure Q3 c)

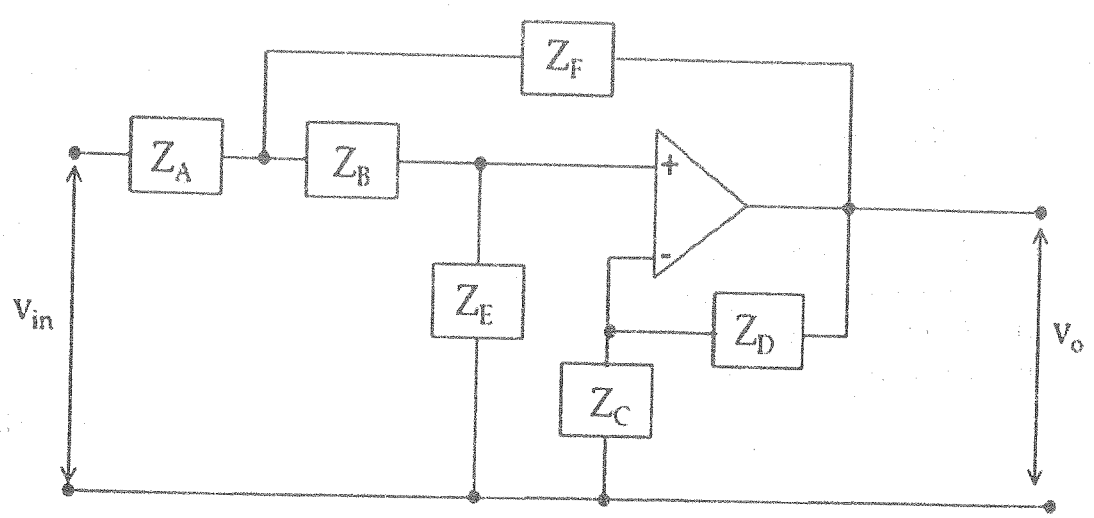

Figure Q3 e)

Table 1

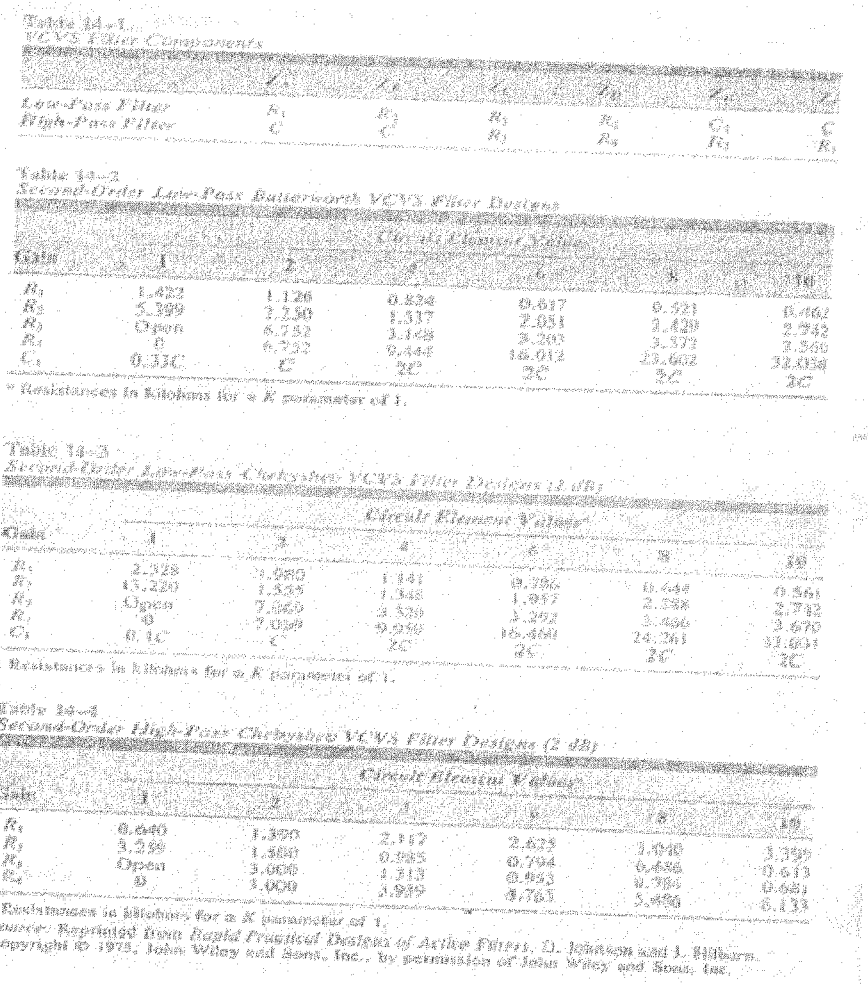

Table 14-1
VCVS Filter Components

	F_0	F_1	F_2	F_3	F_4	F_5
Low-Pass Filter	R_1	R_2	R_3	R_4	C_1	C
High-Pass Filter	C	C	R_1	R_4	R_1	R_1

Table 14-2
Second-Order Low-Pass Butterworth VCVS Filter Designs

	Circuit Element Values*					
Gain	1	2	3	4	5	10
R_1	1.482	1.126	0.824	0.617	0.521	0.462
R_2	5.399	3.250	1.317	2.051	1.429	2.942
R_3	Open	6.752	3.148	3.203	3.572	3.240
R_4	0	6.752	9.444	16.012	25.002	32.059
C_1	0.33C	C	2C	3C	5C	2C

* Resistances in kilohms for a K parameter of 1.

Table 14-3
Second-Order Low-Pass Chebyshev VCVS Filter Designs (3 dB)

	Circuit Element Values*					
Gain	1	2	3	4	5	10
R_1	2.328	1.080	1.141	0.796	0.644	0.561
R_2	15.220	1.535	1.348	1.917	2.336	2.742
R_3	Open	7.065	3.529	3.252	3.496	3.670
R_4	0	7.059	9.256	16.460	24.261	31.603
C_1	0.1C	C	2C	2C	3C	2C

* Resistances in kilohms for a K parameter of 1.

Table 14-4
Second-Order High-Pass Chebyshev VCVS Filter Designs (3 dB)

	Circuit Element Values*					
Gain	1	2	3	4	5	10
R_1	0.640	1.390	2.197	2.623	3.040	3.359
R_2	3.299	1.380	0.985	0.794	0.488	0.613
R_3	Open	3.000	1.313	0.953	0.795	0.681
R_4	0	1.000	3.939	6.765	5.456	6.133

* Resistances in kilohms for a K parameter of 1.

Source: Reprinted from Rapid Practical Designs of Active Filters, D. Johnson and J. Hilburn.
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Q4 a) i) Draw a circuit based on a single operational amplifier to subtract two signals V_1 and V_2 and formulate an expression for the output V_o.

ii) Give an alternative circuit to perform subtraction of two input signals and demonstrate the subtraction process.

[4 Marks]

b) i) Give an operational amplifier based ideal integrator circuit and demonstrate the integration process.

ii) When the input is sinusoidal, demonstrate how the integrator performs as a filter.

[2.5 Marks]

c) i) Reproduce the circuit for a square wave oscillator based on a single operational amplifier.

ii) Name the circuit in part i).

iii) Explain the square wave generation process for the circuit in part i).

[3.5 Marks]

Q5 a) i) State three differences between Field Effect Transistors (FETs) and Bipolar Junction Transistors (BJTs).

ii) Sketch the structure of a N-channel JFET indicating the terminals and show how it is biased for normal operation.

iii) The self-bias circuit of a N- channel JFET shown in Figure Q5 a) has I_{DSS} = 12 mA and V_P = - 4.5 V. Determine the Q point values of I_D and V_{DS} and show that the Q point is in the pinch-off region.

[4 Marks]

b) i) Show that the trans-conductance (g_m) for a JFET is given by

$$g_m = \frac{2I_{DSS}}{|V_P|}\sqrt{\frac{I_D}{I_{DSS}}} \quad \text{Seimens}$$

Hint:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

ii) The JFET in the common source amplifier configuration shown in Figure Q5 b) has $g_m = 4.2 \times 10^{-3}$ S and $r_d = 98$ kΩ.
Sketch the small signal ac equivalent circuit and calculate the voltage gain.

[4 Marks]

c) i) State the two types of MOSFETs.

ii) Draw the N-channel depletion type MOSFET characteristic curves and indicate all the regions of operation.

iii) Sketch the voltage divider biasing circuit for an enhancement type N-channel MOSFET.

[2 Marks]

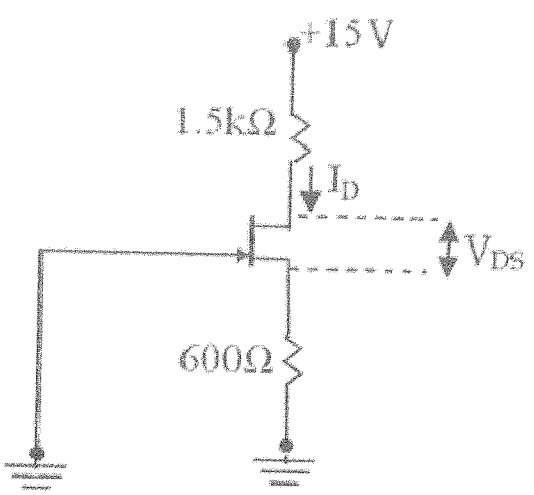

Figure Q5 a)

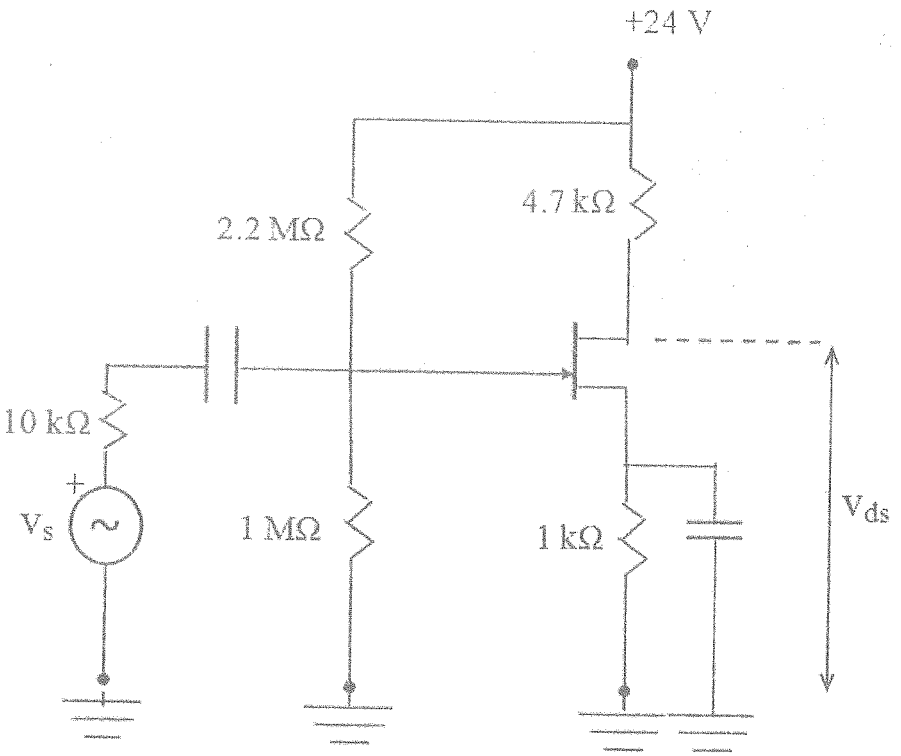

Figure Q5b)