

## UNIVERSITY OF RUHUNA

## Faculty of Engineering

End-Semester 3 Examination in Engineering: July 2016

Module Number: EE3306

(Old Curriculum)

Module Name: Analog Electronics

[Three Hours]

[Answer all questions, each question carries 10 marks]

## All notations have their usual meanings.

Predict that the constant current source I in the circuit in Figure Q1 is mirrored to the Q1 a) collector current of the transistor T2. Assume that T1 and T2 are matched.

[2 Marks]

- Reproduce the circuit of an ideal differential amplifier that has collector bias b) resistors 6 k $\Omega$ , supply voltage +15 V and a constant current source of 2 mA.
  - Calculate the internal emitter resistance of the transistors for this ideal ii) differential amplifier.
  - When the input 2 of the ideal differential amplifier circuit is grounded and a sinusoidal signal is applied to the input 1, calculate the magnitude and phase of the voltages at the
    - I) emitters of the transistors
    - II) output 1
  - When the signals  $\pm$  20 sin ( $\omega t$ ) mV is applied to inputs 1 and 2 respectively, by inference determine the magnitude and phase of the two output voltages.

[6 Marks]

- The CMRR is defined as  $|A_d|/|A_{cm}|$  where  $A_d$  is the output difference voltage caused by common mode signals and Acm the common mode signal respectively.
  - State the meaning of the acronym CMRR. i)
  - When the inputs to a differential amplifier are:  $v_{i1} = 0.1 \sin(\omega t)$  and  $v_{i2} = -0.1 \sin(\omega t)$

the outputs are:  $v_{o1}$  = -5 sin ( $\omega t$ ) and  $v_{o2}$  = 5 sin ( $\omega t$ )

When both inputs are 2 sin (ωt) the outputs are:  $v_{\text{o1}}$  = - 0.04 sin ( $\omega t$ ) and  $v_{\text{o2}}$  = 0.04 (sin  $\omega t$ )

Calculate the CMRR in dB.

[2 Marks]

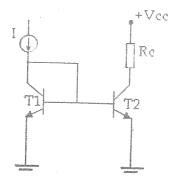


Figure Q1

- Q2 a) Define the properties of an ideal operational amplifier.
  - Draw the circuit of an inverting amplifier based on an operational amplifier. ii)
  - State how the inverting amplifier can be used as a Voltage Follower.
  - Explain briefly how a Voltage Follower can be used practically.

2 Marks

For an operational amplifier b)

- Sketch the desired frequency response of the open loop gain and denote its characteristic features.
- Define the Gain Bandwidth Product (GBP) and the Closed Loop Gain ii) Bandwidth (BWCL) in terms of the GBP.
- iii) Define the slew rate.
- For a sinusoidal output  $V_o(t) = K \sin(\omega t)$ , predict the maximum frequency permitted by the slew rate.

[2.5 Marks]

- For the inverting amplifier in part a), a resistor R<sub>c</sub> can be connected in series with the c) non-inverting input in order to minimize the input offset current.
  - Formulate an expression for the value of R<sub>c</sub>.
  - Show that the output offset voltage due to bias currents are minimized when the ii) input bias currents  $I_B$ <sup>+</sup> and  $I_B$ - are equal.
  - Describe the origin of the input offset voltage and formulate an expression for iii) the output offset voltage due to the input offset voltage.
  - Express the total output offset voltage for the worst case from the derived iv) expressions.
  - State how the output offset voltage is minmized in practice. V)

[5.5 Marks]

- Q3 a) State the difference between an oscillator and a multivibrator.
- [0.5 Marks]
- Sketch a block diagram of an oscillator and state the necessary conditions for b) oscillation.
- Figure Q3 c) shows the Colpitts oscillator circuit.  $R_1 >> X_{C2}$  where  $X_{C2}$  is the reactance C) of C2. Determine the oscillating frequency of the circuit and the gain required for the amplifier.
- Explain the difference between a Butterworth and a Chebyshev filter considering d) their frequency responses.
- [1 Mark] Using the data in Table 1 and the circuit in Figure Q3 e), design a second-order low e) pass Butterworth filter with a cut-off frequency 2.5 kHz and a gain in the passband of 2. The constant  $K = 10^4/(fC)$  where f is the desired cut-off frequency in Hz and C is the value of capacitance selected in Farads.

[3.5 Marks]

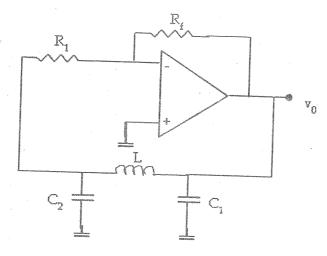


Figure Q3 c)

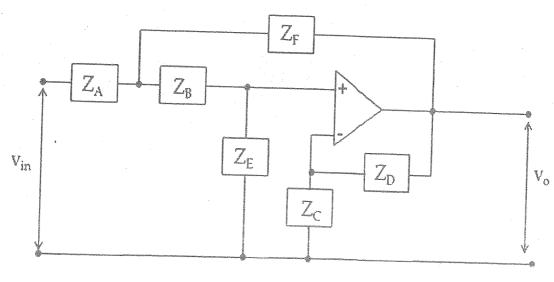


Figure Q3 e)

## Table 1

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- Draw a circuit based on a single operational amplifier to subtract two signals  $V_1$ Q4 a) i) and  $V_2$  and formulate an expression for the output  $V_o$ .
  - Give an alternative circuit to perform subtraction of two input signals and ii) demonstrate the subtraction process.
  - [4 Marks] Give an operational amplifier based ideal integrator circuit and demonstrate the b) i) integration process.
    - When the input is sinusoidal, demonstrate how the integrator performs as a ii) filter.

[2.5 Marks]

- Reproduce the circuit for a square wave oscillator based on a single operational c) i) amplifier.
  - Name the circuit in part i). ii)
  - Explain the square wave generation process for the circuit in part i).

[3.5 Marks]

Acores: Reprinted from Espirit Tractical Designs of Arrive Filters. D. Johnson and J. Hilburn. Copyright S 1975, John Wiley and Sons, Inc., by permission of John Wiley and Sons, Inc.

- Q5 a) i) State three differences between Field Effect Transistors (FETs) and Bipolar Junction Transistors (BJTs).
  - ii) Sketch the structure of a N-channel JFET indicating the terminals and show how it is biased for normal operation.
  - iii) The self-bias circuit of a N- channel JFET shown in Figure Q5 a) has  $I_{DSS} = 12 \text{ mA}$  and  $V_P = -4.5 \text{ V}$ . Determine the Q point values of  $I_D$  and  $V_{DS}$  and show that the Q point is in the pinch-off region.

[4 Marks]

b) i) Show that the trans-conductance  $(g_m)$  for a JFET is given by

$$g_m = \frac{2I_{DSS}}{|V_P|} \sqrt{\frac{I_D}{I_{DSS}}}$$
 Seimens

Hint:

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

- ii) The JFET in the common source amplifier configuration shown in Figure Q5 b) has  $g_m = 4.2 \times 10^{-3} \, \text{S}$  and  $r_d = 98 \, \text{k}\Omega$ . Sketch the small signal ac equivalent circuit and calculate the voltage gain.
- c) i) State the two types of MOSFETs.

[4 Marks]

- ii) Draw the N-channel depletion type MOSFET characteristic curves and indicate all the regions of operation.
- iii) Sketch the voltage divider biasing circuit for an enhancement type N- channel MOSFET.

[2 Marks]

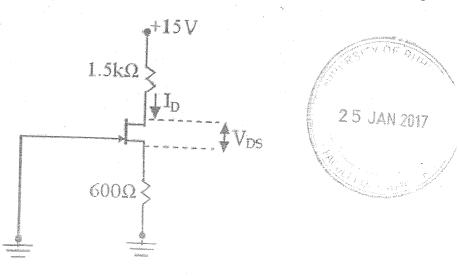


Figure Q5 a)

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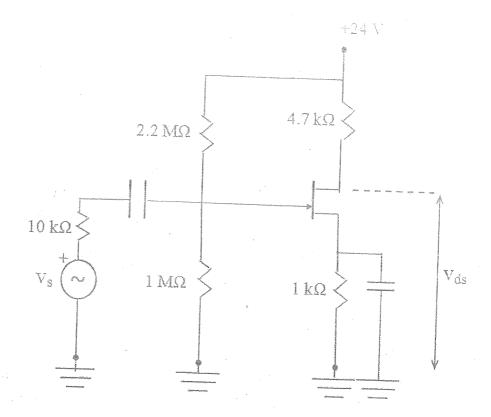


Figure Q5b)