UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5 Examination in Engineering: July 2016

Module Number: EE5208 **Module Name: Electronics Circuit Design**

[Three Hours]

[Answer **all questions**, each question carries **10 marks**]

Q1 a) Explain the difference between passive circuit elements and active circuit elements. [1.0 Mark]

b) A typical Zener regulator is shown in Figure Q1 b). The tolerance of R is ± 6%. Input voltage V_{in} = 12 V ± 5% and the output voltage V_o = 7 V ± 5%.
Suppose you are given two Zener diodes having the rated values as shown in Table Q1 b).
The maximum load current should be kept at 120 mA while the minimum is 0 mA.

Table Q1 b)

Zener Diode	Rated Voltage	Rated Power
Z1	7.5 V	1.5 W
Z2	7.5 V	0.5 W

i) Select a suitable Zener diode from Z1 and Z2. State any assumptions you make.
ii) Determine the value of R from E12 series.

[5.0 Marks]

c) A voltage divider circuit is shown in Figure Q1 c). R_1 = 1 kΩ Tolerance values for the resistances are 5%. Input voltage V_{in} = 80 V. Select a suitable value for R_2 in E12 series such that 55 V ≤ V_0 ≤ 62 V.

[4.0 Marks]

Q2 a) A PCB (Printed Circuit Board) provides both a physical structure for mounting and holding electronic components and the electrical interconnection between components.
i) Classify PCBs according to their use in applications.
ii) State the two types of double sided PCBs.
iii) Sketch the configuration of a plated through hole.
iv) List the basic PCB design steps.

[3.0 Marks]

b) The process of removing metal from the surface of a PCB by chemical dissolution is called Etching.
i) Briefly explain two types of etching techniques with relevant sketches.
ii) State what is meant by "Overhang" in etching.

[2.0 Marks]

c) A basic low pass filter circuit design is shown in Figure Q2 c). Show that

$$\frac{V_{out}}{V_{in}} = \frac{1}{j\omega CR}$$

and hence determine the filter transfer function in the S domain.

[1.5 Marks]

d) Design a third-order unity gain Bessel high pass non-inverting filter with cut-off frequency f_c = 3 kHz. Use the Table Q2 d). Given that, i = 1, 2.

Table Q2 d)

Type	a_i	b_i	Capacitance
Filter 1	$a_1 = 0.7560$	$b_1 = 0.0000$	100 nF
Filter 2	$a_2 = 0.9996$	$b_2 = 0.4772$	100 nF

[3.5 Marks]

Q3 a) A filter is a device that can be defined as a frequency selective circuit.

i) State the two types of analog filters. Briefly explain them.

ii) Sketch a practical high pass filter response curve and indicate the pass band and the stop band.

iii) Briefly explain three types of active filter design techniques.

[3.0 Marks]

b) Give first order low pass filter design circuits for the Inverting and non-Inverting cases and state the Transfer functions for them.

[2.0 Marks]

c) Design a 5th-order unity-gain Butterworth low pass filter with cutoff frequency f_c = 100 kHz using Sallen-Key topology. Capacitance values for the filters are shown in Table Q3 c). Design each partial filter and draw it as a combination by specifying the capacitor values and calculating the required resistor values. Make necessary assumptions if required.

Table Q3 c)

Type	a_i	b_i	Capacitance
Filter 1	$a_1 = 1.0000$	$b_1 = 0.0000$	22 nF
Filter 2	$a_2 = 1.6180$	$b_2 = 1.0000$	820 pF
Filter 3	$a_3 = 0.6180$	$b_3 = 1.0000$	150 pF

[5.0 Marks]

Q4 a) i) State two differences between a Depletion type N-MOSFET (N-Channel Metal Oxide Semiconductor Field Effect Transistor) and an Enhancement type N-MOSFET.

ii) Sketch the structure of an Enhancement type N-MOSFET showing the DC biasing for normal operation.

iii) Reproduce the Enhancement type N-MOSFET drain and transfer characteristics and indicate the different regions of the curve.

[3.0 Marks]

b) i) Prove that the trans-conductance (g_m) for an Enhancement type N-MOSFET is given by,

$$g_m = \beta(V_{GS} - V_T) \text{ Siemens}$$

Hint: Use the transfer characteristic curve sketched in Q4 a) iii).

ii) The Enhancement type N-MOSFET in the circuit shown in Figure Q4 b) has the following parameters.
$V_T = 2.5$ V, $\beta = 0.6 \times 10^{-3}$ A/V^2, $r_d = 80$ kΩ and $g_m = 1.2 \times 10^{-3}$ S.

I. Verify that the N-MOSFET is biased in its active region.
II. Calculate the input resistance of the N-MOSFET.
III. Draw the small-signal ac equivalent circuit and determine the overall voltage gain V_L / V_s.

[5.0 Marks]

c) An Enhancement MOSFET can be used as a nonlinear resistor by joining the Gate and the Drain terminals together.
If the drain characteristic of such a MOSFET is given by,

$$I_D = 0.5\beta(V - V_T)^2, \quad V > V_T$$
$$I_D = 0, \quad V \le V_T$$

show that the small signal ac resistance is

$$r = \frac{1}{\sqrt{2\beta I}}$$

and the DC resistance is

$$R = \sqrt{\frac{2}{\beta I}} + \frac{V_T}{I}$$

where I denotes the current.

[2.0 Marks]

Q5 a) Briefly explain the following methods used to express the relationship between a logic circuits inputs and outputs.
i) Logical statement in our own language
ii) IEEE/ANSI standard logic symbols
iii) Text based language description

[1.5 Marks]

b) The chip design flow is a conceptual design flow from specifications to final product.
i) Draw a flow chart to show the chip design flow.
ii) Briefly explain each step involved in chip design flow.

[3.0 Marks]

c) A hardware description language (HDL) is a computer-based language that describes the hardware of digital systems in a textual form. Verilog can be identified as an example of HDL.

i) The system shown in Figure Q5 c) consists of five modules namely Mux, Alu, Shift, Q_reg and R_reg. Using the description given below, write Verilog codes for modules Mux, Alu and Q_reg. Assume all inputs are single bit unless otherwise mentioned.

Module Mux has two inputs (B and R) and one output (M). If input B is digital 1, then output M = B. Otherwise M = R (Output of R_reg)
Alu has three inputs (A, M and ALU_OP) and one output (X).
ALU_OP is a three bit variable that describes different mathematical functions shown in Table Q5 c).

Hint: Use if or case statements.
Q_reg has one input(S) and one output (Q). It is a register that stores the value of an input and gives an output at the positive edge of the next clock cycle.

Table Q5 c)

ALU_OP	Operation
000	A
001	A+M
010	A-M
011	M-A
100	-(A+M)
101	A and M
110	A or M
111	A xor M

ii) Include Mux, Alu and Q_reg in a top module and write a test bench for the top module.

[5.5 Marks]

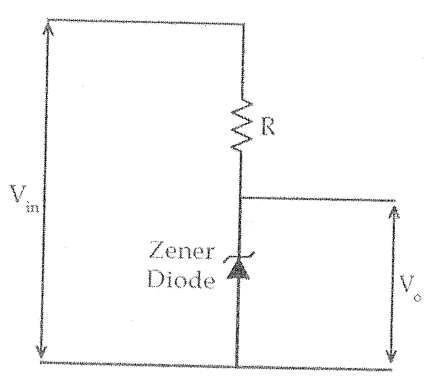

Figure Q1 b)

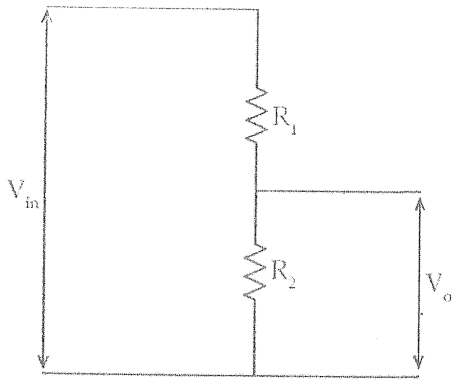

Figure Q1 c)

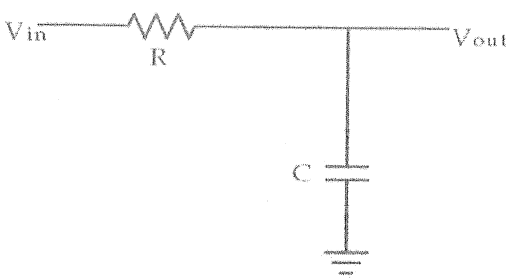

Figure Q2 c)

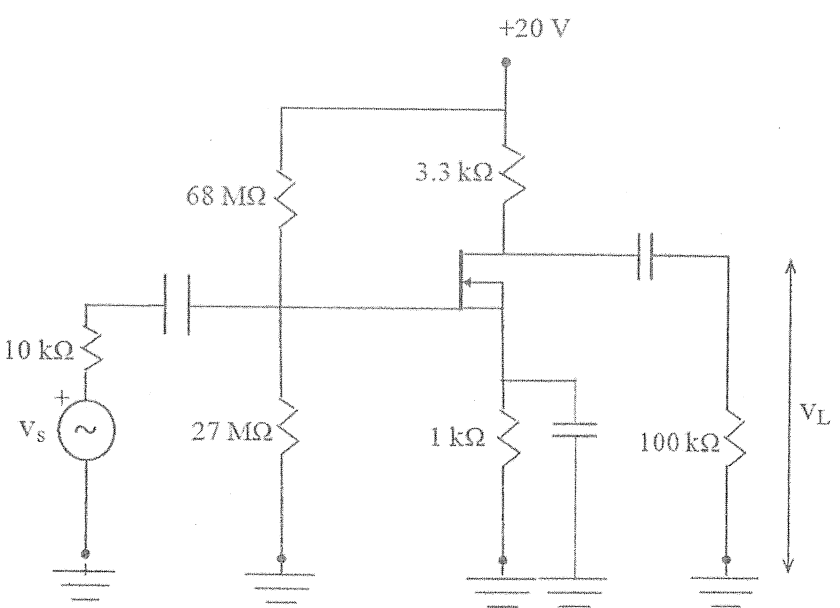

Figure Q4 b)

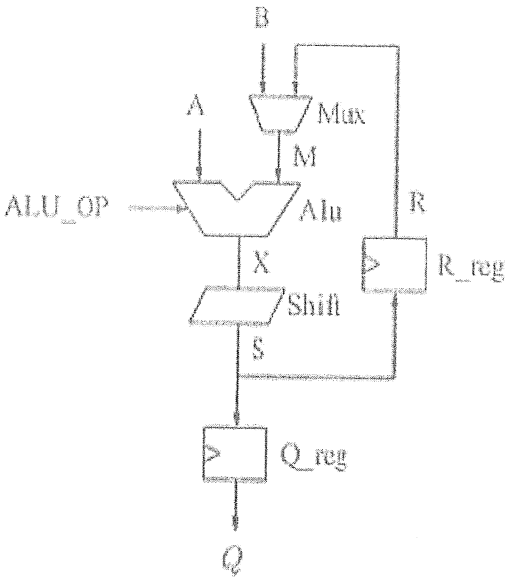

Figure Q5 c)