UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 4 Examination in Engineering: December 2016

Module Number: EE4204

Module Name: Electrical and Electronic Measurements

[Three Hours]

[Answer **all questions**, each question carries **10 marks**]

Q1 a) i) Sketch the basic construction of a cathode-ray-tube (CRT) oscilloscope.
ii) Identify the basic sections of the CRT and explain briefly the operation of each section.

[3 Marks]

b) A 2 kHz triangular wave with peak amplitude 10 V is applied to the vertical deflecting plates of a CRT. A 1 kHz Sawtooth wave with peak amplitude 20 V is applied to the horizontal deflecting plates. The CRT has a vertical deflection sensitivity of 0.4 cm/V, and a horizontal deflection sensitivity of 0.25 cm/V. Assuming that the two inputs are synchronized, determine the waveform display on the screen.

[4 Marks]

c) Briefly explain pre-triggering, post triggering, baby-sitting mode and roll mode in a Digital Storage Oscilloscope (DSO).

[3 Marks]

Q2 a) Sketch the Lissajous patterns for a sine wave of 75 Hz applied to the vertical deflection plates of an oscilloscope when the following signals are applied at the horizontal deflection plates.

i) 150 Hz
ii) 50 Hz
iii) 75 Hz with 90° phase difference
iv) 75 Hz with 45° phase difference

[3 Marks]

b) A source with signal amplitude 750 mV and source resistance 1 kΩ is connected to an oscilloscope which has an input impedance of 1 MΩ in parallel with a capacitance of 40 pF. A coaxial cable with a 1:1 probe with 80 pF capacitance is used for connecting the source to the oscilloscope.

i) Calculate the signal voltage level (V_i) at the oscilloscope terminals when the signal frequency is 120 Hz.
ii) Calculate the signal frequency at which V_i is 3 dB below supply voltage.

[4 Marks]

c) i) Draw the block diagram of a Swept Superheterodyne Spectrum Analyzer.
ii) Using the diagram you have drawn, briefly discuss the operating principle of the Swept Superheterodyne Spectrum Analyzer.

[3 Marks]

Q3 a) A permanent magnet moving coil (PMMC) instrument with Full Scale Deflection (FSD) = 100 μA and R_m = 1 kΩ is to be employed as a full wave rectifier ac voltmeter with FSD = 100 V_{rms}. Silicon diodes (voltage drop 0.7 V) are used in the bridge rectifier circuit in Figure Q3.

i) Calculate the multiplier resistance value required.

ii) Calculate the pointer indications for the voltmeter, when the rms input voltage is

I) 75 V

II) 50 V

iii) Calculate the sensitivity of the voltmeter at FSD.

[5 Marks]

b) i) Draw the circuit diagram of a fundamental suppression harmonic distortion analyzer.

ii) Briefly describe the operation of a rejection amplifier.

iii) Sketch the frequency response of a fundamental suppression analyzer

[3 Marks]

c) Draw the circuit diagram of a Digital Frequency Counter and briefly explain the operation of the time base generator unit.

[2 Marks]

Q4 a) Write short notes on the following terms,

i) Static and Dynamic performance characteristics

ii) Zero Drift

iii) Accuracy and precision

iv) Dynamic Error

[4 Marks]

b) Two currents (I_1 and I_2) from different sources flow in opposite directions through a resistor. I_1 is measured as 79 mA on a 100 mA analog instrument with an accuracy of ±3% of full scale. I_2 determined as 31 mA, is measured on a digital instrument with ±100 μA accuracy. Calculate the maximum and minimum levels of the current in the resistor.

[3 Marks]

c) The voltages at opposite ends of a 470 Ω ±5% resistor (R) are measured as, V_1 =12 V and V_2 =5 V. The measuring accuracies are ±0.5 V for V_1 and ±2% for V_2.

i) Calculate the level of current (I) in the resistor, and specify its accuracy.

ii) Determine the maximum and minimum power dissipation in the resistor (Hint: Use $P=I^2R$ to calculate the power).

[3 Marks]

Q5 a) i) State three functions of a Logic Analyzer different from a Digital Oscilloscope.

ii) State which instrument you would use if you want good amplitude resolution and time resolution in a measurement.

iii) Illustrate the conceptual model of a Logic Analyzer with a block diagram.

[2 Marks]

b) i) State what is meant by the acronyms SUT, CLK, LTA, LSA and VLSI.
ii) State the main difference between a LTA and LSA?
iii) The Logic Analyzer probes that interface with the SUT must meet special requirements. State two requirements of the probes.

[2 Marks]

c) i) Explain how a LTA acquisition can have a maximum uncertainty of one sample.
ii) A LTA acquisition is described by the binary sequence 0110100000000010. If the sampling rate is 4 ns
I) Sketch a timing diagram and number the sampling points.
II) How many samples are required to represent the signal?
III) Show the Transition Sampling acquisition for I).
IV) What is the saving in memory by using Transition Sampling in c)?

[4 Marks]

d) Table Q5 gives a LSA listing display for 4 channels.
i) Sketch the LTA timing diagrams.
ii) Show the LSA acquisition in the LTA timing diagrams.

[2 Marks]

Table Q5

Sample	Counter (H)	Timestamp
0	7	0 ns
1	C	100 ns
2	5	200 ns
3	A	300 ns
4	F	400 ns
5	8	500 ns
6	4	600 ns
7	C	700 ns

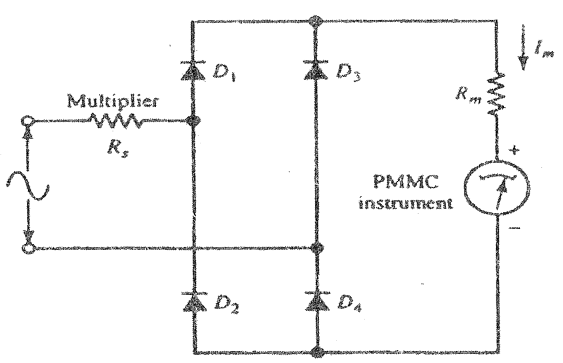

Figure Q3