UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 6 Examination in Engineering: January 2022

Module Number: EE6205 **Module Name: Hardware Description Language**

[Three Hours]

[Answer **all questions**, each question carries **10** marks]

Q1 a) i) Briefly explain the major difference between FPGA and standard cell-based ASICs.

[1.0 Marks]

ii) Organize the steps in the following list to show the proper execution order of the ASIC-frontend flow.
[Clock tree synthesis, Placement, floor planning, power planning, Routing]

[1.0 Marks]

b) i) Briefly explain what the drive strength of a logic gate is and its impact on timing paths

[1.0 Marks]

ii) Consider a NMOS transistor whose drive strength is D. If the width of the gate and the length of the transistor are doubled while keeping all the other factors constant, evaluate the new drive strength of the transistor.

[1.0 Marks]

c) i) Draw a proper timing diagram and briefly explain the propagation delay of a logic gate.

[1.5 Marks]

ii) Table Q1 lists an excerpt of a test.lib file which comes with a technology library named 'TEST'. Use the table to calculate the value of the output slew of the logic gate when the input slew is 0.7 ns and output load is 2 pF. Assume all the output slews in the table are in ns

```
rise_transition("template1") { /* Output slew on Q*/
  index_1 ("0.02, 0.5, 1.0, 4.0"); /* Range of output load */
  index_2 ("0.01, 0.5, 0.9, 1.3, 2.5"); /* Range of input slew */
  values ("0.1, 0.2, 0.3, 0.4, 0.5",\
          "1.1, 1.2, 1.3, 1.4, 1.5",\
          "2.1, 2.2, 2.3, 2.4, 2.5",\
          "3.1, 3.2, 3.3, 3.4, 3.5");
  }
```

Table Q1

[2.0 Marks]

d) Derive an expression to calculate the slack (in Nano seconds) for a setup analysis for the circuit shown in Figure Q1 in terms of T_{buf}, T_{combo}, F_{clk}, T_{cq}, T_s and T_{su}.

- Delay of a single buffer in clock tree is T_{buf} ns and all the buffers are identical.
- Frequency of the clock, clk, is F_{clk} GHz
- Delay across the combinational data path is T_{combo} ns
- Clock to Q delay of flip-flops is T_{cq} ns
- Setup time of flops is T_s ns
- Setup uncertainty is T_{su} ns

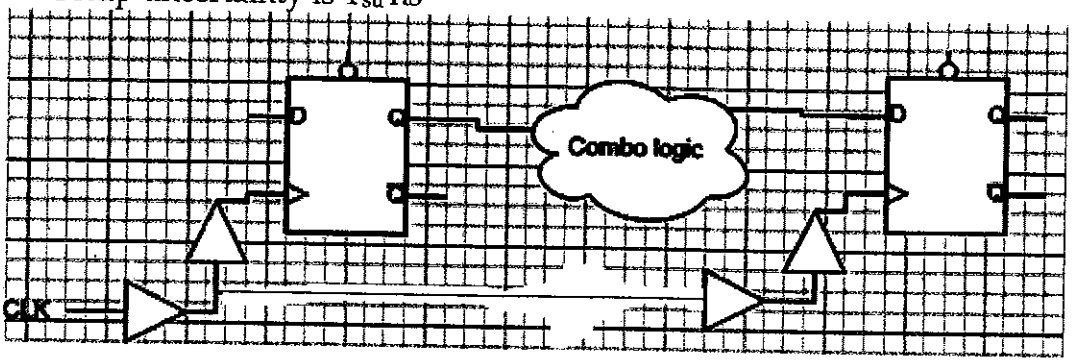

Figure Q1

[2.5 Marks]

Q2 a) i) Briefly explain the difference between blocking and non-blocking assignments in Verilog.

[1.0 Marks]

ii) Write a small code fragment in Verilog to synthesize a single-bit tri-state buffer.

[1.5 Marks]

b) i) Construct a **Moore** machine to output the value '1' as it detects the sequence '110'.

[1.5 Marks]

ii) Determine the number of D flip-flops required to design the above state machine if you use binary encoding to encode states?

[1.0 Marks]

iii) Write a Verilog statement using 'reg' data type and a variable name called 'current_state' to represent all the flip-flops that are required for your state machine.

[1.0 Marks]

iv) Write Verilog 'if-else' statement to show the behavior of the state machine at the initial state.

[1.0 Marks]

v) Write Verilog code to show how to set the output of the state machine as state changes. (You need to use 'always' block and case statements in Verilog. Also, you may name your states as S0, S1,....and so on.)

[1.0 Marks]

c) Draw the timing diagram to show the simulation result for the test bench given below in Figure Q2.

[2.0 Marks]

```
`timescale 100ps/1ps

module examtb ();
reg ca,cb;

initial begin
   ca = 1'b1;
   cb = 1'b1;

   #30 cb = 1'b0;
   #10 ca = 1'b0;
end

always begin
   #10 cb = ~cb ;
   #10 ca = ~ca ;
end


initial
#150 $finish;

endmodule
```

Figure Q2

Q3 a) i) Though gray encoding is suitable to synchronize the control bus signals as they cross different clock domains, gray encoding is not appropriate to synchronize data buses. Briefly explain the reason behind the above statement.

[1.5 Marks]

ii) Mention two techniques that can be used to synchronize data buses.

[1.0 Marks]

iii) Consider the clock domain crossing takes place in between flop A and flop B as shown in the Figure Q3. Timing diagrams of the two clock signals C1 and C2 are also shown in the figure. Copy the timing diagram of C1 and C2 to your answer sheet and draw the possible timing diagrams for A and B nets (which are the output nets of source flop and destination flop, respectively) with respect to the clock signals when the input sequence for the source flop is '00101111'. Hence, identify a data loss.

[2.5 Marks]

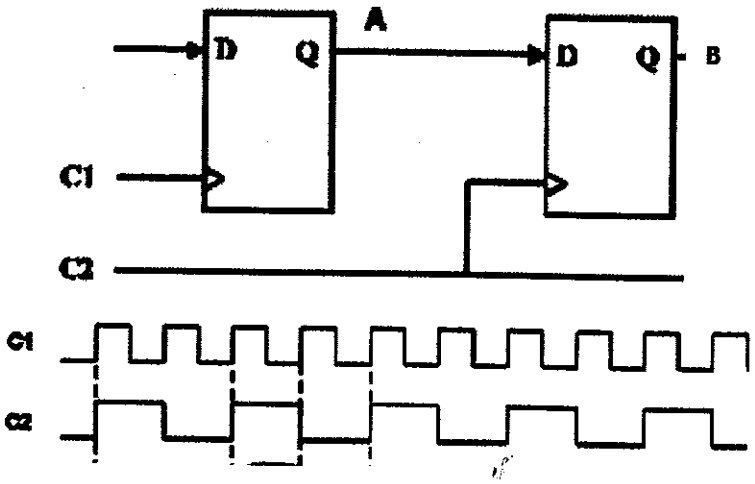

Figure Q3

b) i) Briefly explain the switching power dissipation in CMOS circuits.

[1.0 Marks]

ii) State two factors on which switching power dissipation depends on.

[1.0 Marks]

iii) Clock gating can be used to reduce the switching power dissipation of a digital circuit. Draw a proper circuit diagram to illustrate the clock gating concept.

[1.0 Marks]

iv) List two types of major power dissipation mechanisms in CMOS circuits apart from the switching power dissipation.

[1.0 Marks]

v) Briefly explain one of the power dissipation mechanisms that you have mention in above (iv).

[1.0 Marks]

Q4 a) i) Compare VHDL and Verilog languages in terms of case sensitivity and user defined data types.

[1.5 Marks]

ii) Briefly explain the usage of STD_LOGIC type in VHDL.

[1.0 Marks]

b) Draw a basic digital circuit diagram to show the synthesized output of the VHDL code given in Figure Q4.

[3.5 Marks]

```
library ieee;
use ieee.std_logic_1164.all;
-- entity declaration
entity even_detector is
  port(
      a: in std_logic_vector(2 downto 0);
      even: out std_logic
  );
end even_detector;
-- architecture body
architecture sop_arch of even_detector is
  signal p1, p2, p3, p4 : std_logic;
  begin
  even <= (p1 or p2) or (p3 or p4);
  p1 <= (not a(2)) and (not a(1)) and (not a(0));
  p2 <= (not a(2)) and a(1) and a(0);
  p3 <= a(2) and (not a(1)) and a(0);
  p4 <= a(2) and a(1) and (not a(0));
end sop_arch;
```

Figure Q4

c) i) Write a 2-input Multiplexer in VHDL language.

[2.0 Marks]

ii) Write a simple D flip-flop which has a data input (D), clock input (Clk) and output (Q) in VHDL language.

[2.0 Marks]

Q5 a) Draw the internal structure of a 2-input look up table (LUT) of a FPGA. (You may draw the registers, 2- input multiplexers, and input and output ports appropriately).

[3.0 Marks]

b) i) Identify the types of projects and product developments, usage of FPGAs is better than usage of ASICs?

[1.0 Marks]

ii) Briefly explain how the RTL synthesis for FPGA device differs from the RTL synthesis for an ASIC device.

[1.5 Marks]

iii) State two factors that need to be considered when choosing a FPGA for your design.

[1.0 Marks]

c) i) Draw the internal structure of a FPGA Configurable logic block (CLB) having a look up table, a multiplexor, and a D Flip-flop

[1.0 Marks]

ii) Draw a simple diagram to show the internal structure of a FPGA switch box having 6 MOSFET switches.

[1.0 Marks]

iii) Briefly explain the role of CLBs and switch boxes in synthesizing digital logic in FPGA.

[1.5 Marks]

-End of Exam Paper-