UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 4 Examination in Engineering: December 2015

Module Number: EE4302 **Module Name: Digital Electronics**

[Three Hours]

[Answer **all questions**, each question carry 10 marks]

Q1 a) Explain the difference between Minterms and Maxterms in relation to Sum-of-Products (SoPs) and Product-of-Sums (PoSs) Boolean expressions.

[1.5 Marks]

b) Use the minterm expansion of f and the maxterm expansion of g and determine whether $f = g$

$f(a,b,c,d) = bc + \bar{a}\bar{d} + a\bar{b}\bar{c} + \bar{b}\bar{c}\bar{d}$

$g(a,b,c,d) = (\bar{a} + \bar{b} + c)(a + b + \bar{d})(\bar{b} + c + \bar{d})(\bar{a} + b + \bar{c})$

[2.5 Marks]

c) Show that NAND and NOR gates are both functionally complete.

[1.0 Mark]

d) A switching network has two control inputs C_1, C_2, two data inputs D_1, D_2 and one output Z.

If $C_1 = C_2 = 0$, the output is $Z = 0$

If $C_1 = C_2 = 1$, the output is $Z = 1$

If $C_1 = 1$ and $C_2 = 0$, the output is $Z = D_1$

If $C_1 = 0$ and $C_2 = 1$, the output is $Z = D_2$

i) Derive the truth table for Z

ii) Use a Karnaugh map to minimize the expression of Z

iii) Implement the switching network using only NAND gates.

[5.0 Marks]

Q2 a) What is the difference between a synchronous counter and an asynchronous counter?

[1.5 Marks]

b) A special clocked Master-Slave flip-flop that has two inputs M and N, operates as follows.

If $MN = 00$, the next state of the flip-flop output is 1

If $MN = 01$, the next state of the flip-flop output is the same as present.

If $MN = 10$, the next state of the flip-flop output is the complement of present.

If $MN = 11$, the next state of the flip-flop output is 0

Complete the transition table shown in Table Q2 for the above flip-flop. Use Don't Care states if required.

[2.5 Marks]

c) Using the flip-flop in part b), design a counter that counts through the sequence 000, 100, 110, 111, 011, 001, 000

[6.0 Marks]

Q3 a) Explain how a sequential logic circuit can be represented by using a state table and a state diagram.

[1.5 Marks]

b) Obtain the truth table of a basic NOR SR flip-flop.

[2.5 Marks]

c) A synchronous sequential circuit is shown in Figure Q3.

i) Derive the state table of the synchronous sequential circuit.

ii) Are there any equivalent states identifiable by inspection?

iii) Use the implication table method to show that this sequential circuit can be reduced to no more than four states.

iv) Make a state assignment to the reduced state table ensuring that the next state(s) of a certain state is/are made adjacent to the original state.

v) What is the purpose of having state G in the original state diagram?

[6.0 Marks]

Q4 a) What is demultiplexing in digital logic circuit design?

[1.5 Marks]

b) Determine the Boolean expressions for the outputs of a 1×4 demultiplexer.

[3.5 Marks]

c) i) Draw the circuit diagram of a basic Diode-Transistor Logic (DTL) NAND gate.

ii) Explain the operation of the DTL NAND gate for any low input and when all the inputs are high.

[5.0 Marks]

Q5 a) i) Explain the operation of a totem-pole two input Transistor-Transistor Logic (TTL) NAND gate.

ii) What is the improvement made with this totem-pole TTL NAND gate compared to a basic TTL NAND gate?

[4.0 Marks]

b) State the criteria for the gate-source voltage of n- and p-channel MOSFETs.

[2.0 Marks]

c) i) Draw the circuit diagram of a two input Complementary MOS (CMOS) NOR gate.

ii) Explain the operation of this two input CMOS NOR gate.

[4.0 Marks]

Table Q2 : Transition table.

Present State (Q_t)	Next State (Q_{t+1})	M	N
0	0		
0	1		
1	0		
1	1		

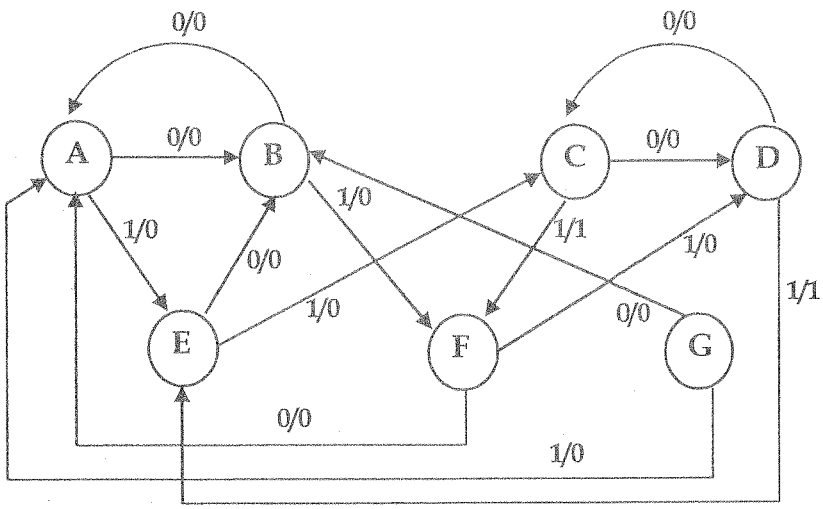

Figure Q3 : State diagram.