UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5 Examination in Engineering: August 2015

Module Number: EE5208 **Module Name: Advanced Electronics**

[Three Hours]

[Answer all questions, each question carries 10 marks]

Q1 a) Explain the cooling methods used in power transistor applications.

[1.5 Marks]

b) A power transistor has maximum rated power dissipation of 5 W at 50 °C case temperature. The thermal resistance from case to ambient is 5 ^{0}C/W.

i) Can the transistor be operated at 5 W of dissipation, without auxiliary cooling when the ambient temperature is 40 °C?

ii) What is the maximum permissible dissipation with no auxiliary cooling, at 40°C ambient?

[3.0 Marks]

c) i) Starting from the equations given below, find the heat sink-ambient thermal resistance R_{sa} for heat sink which is shown in Figure Q1 by considering radiation and convention.

Assume temperature of heat sink (T_s) is 120 ^{0}C and ambient temperature (T_a) is 20 ^{0}C.

Radiated power, P_{RAD} $= 5.1A\left[\left(\frac{T_S}{100}\right)^4 - \left(\frac{T_a}{100}\right)^4\right]$

Power loss due to convention, P_{CONV} $= 1.34A\left[\frac{(T_s - T_a)^{1.25}}{(d_{vert})^{0.25}}\right]$

Where A is effective area and d_{vert} is vertical height of the body.

ii) Find the equivalent thermal resistance in part c) i).

[5.5 Marks]

Q2 a) i) Draw practical low pass filter response curve.

ii) Note down 3 different types of filters and compare those filters characteristics.

[2.0 Marks]

b) i) Briefly explain sallen key topology and multiple feedback topology

ii) Briefly explain quality factor for the band pass and low pass filter

[2.0 Marks]

c) i) List two advantages and two disadvantages of active filters compared to passive filters.

ii) A low pass Butterworth filter circuit design based on a non-inverting amplifier is shown in Figure Q2. Show that,

$$V_1 = \frac{V_{in}}{1+j\omega RC}$$

$$\frac{V_0}{V_{in}} = \frac{A_f}{1+j\left(\frac{f}{f_c}\right)}$$

$$If\ \omega = 2\pi f,\quad f_c = \frac{1}{2\pi RC}$$

$$A_f = 1 + \frac{R_f}{R_1}$$

iii) The task is to design a fifth-order unity-gain Butterworth low-pass filter with the corner frequency fc = 50 kHz.

Table Q2 c)

	a_i	b_i	Capacitance
Filter 1	a_1 =1	b_1 = 0	1 nF
Filter 2	a_2 =1.6180	b_2 = 1	820 pF
Filter 3	a_3 =0.6180	b_3 = 1	330 pF

Capacitance values for the filters are shown in above table. Dimension the each partial filter by specifying the capacitor values and calculating the required resistor values. Take necessary assumption if it is required.

[6.0 Marks]

Q3 a) The circuit shown in Figure Q3 (a) is a part of a power supply circuit. The specifications of the circuit are given bellow. Note that all the symbols have their usual meaning. Find the suitable value for R_1 and R_2 in E12 series.
Tolerance value for R_1 and R_2 is 5%.

$$R = 1K\Omega \pm 5\%$$
$$V_{in} = 30V \pm 5\%$$
$$V_0 = 12V \pm 5\%$$
$$I_{L,max} = 5\ mA$$
$$I_{L,min} = 0\ A$$

The Zener diodes rated power and rated voltage are 0.1 W and 12 V respectively at no load condition. (E12 series is -1, 1.2, 1.5, 1.7, 2.2, 2,7, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2)

[5.0 Marks]

b) The two types of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are the depletion type and the enhancement type.

i) Sketch the structure of a depletion type N-channel MOSFET (NMOSFET) showing the DC biasing for normal operation.

ii) Sketch the drain and transfer characteristics for the depletion type NMOSFET.

iii) Why are the equations describing JFET operation valid to describe the operation of a depletion type MOSFET?

[2.0 Marks]

c) Figure Q3 (c) shows the voltage division biased small-signal enhancement NMOSFET amplifier circuit.

i) If the transistor is biased at a drain current value (I_D) 1.93 mA and has a threshold voltage, $V_T = 2$ V, what is the biased voltage V_{DS}?

ii) Show that is in the active region of the NMOSFET.

iii) Give the AC equivalent circuit and show that the overall voltage gain of the amplifier is given by,

$$\frac{V_L}{V_S} = \left[\frac{R_1//R_2}{r_s + R_1//R_2}\right](-g_m)(r_d//R_D//R_L)$$

where g_m is the transconductance and r_d is the drain resistance.

[3.0 Marks]

Q4 a) i) Draw the fixed bias circuits and write the equation for a N-type and a P-type Junction Field Effect Transistor (JFET).

ii) How is the operating point (Q) determined from the transfer characteristics in the two cases?

iii) Draw the circuit and the output voltage characteristic graph of a self-biased N-type JFET.

[2.5 Marks]

b) The transfer characteristics of a self-biased N-type JFET is described by the equation,

$$I_D = I_{DSS}\left\{1 - \left(\frac{V_{GS}}{V_P}\right)\right\}^2$$

where I_D is the drain current, I_{DSS} the saturation current, V_{GS} is the gate to source voltage and V_P, is the pinch-off voltage.

i) State the condition that ensures the JFET is operating in the active region.

ii) Derive an expression for ID at the Q point.

iii) By considering two JFETs that have different transfer characteristics, describe why the operating point of the fixed bias circuit is more stable than the self-bias circuit.

iv) How is the stability improved further by the voltage divider bias circuit?

[5.0 Marks]

c) The circuit for the JFET as an analog switch is shown in Figure Q4.

i) Explain its operation and state the voltages of the ON and OFF states.

ii) If R_D=8 kΩ, R_L = 90 kΩ, the ON resistance of the JFET R_D (ON) = 40 kΩ and the analog input V_{DD}= 80 mV, what are the V_L in the ON and OFF states?

[2.5 Marks]

Q5 a) i) Name three (3) Hardware Description Languages (HDL).

ii) What are the three (3) abstraction levels in Verilog language?

[1.0 Mark]

b) i) Why you need to declare all the Left Hand Side (LHS) variables within an "Always" block as registers?

ii) What is called as the "Sensitivity List" in an "Always block"?

iii) What are the 2 types of sensitivity lists? What are the differences between them?

[4.5 Marks]

c) Draw the synthesized view (layout) of the Digital system relevant to the following Verilog code shown in Figure Q5 c).

[2.0 Marks]

d) Explain the differences between blocking and non-blocking assignments with examples.

[2.5 Marks]

e) Draw the state machine relevant to the given Verilog code module in the Figure Q5 e). Which encoding style is used in this example?

[2.0 Marks]

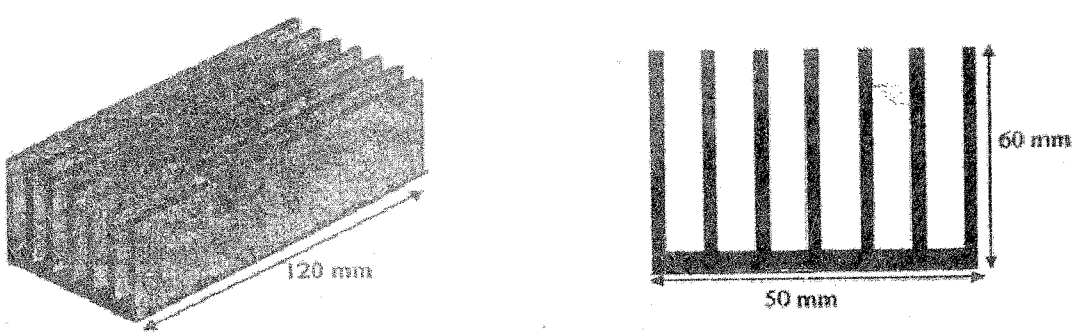


Figure Q1

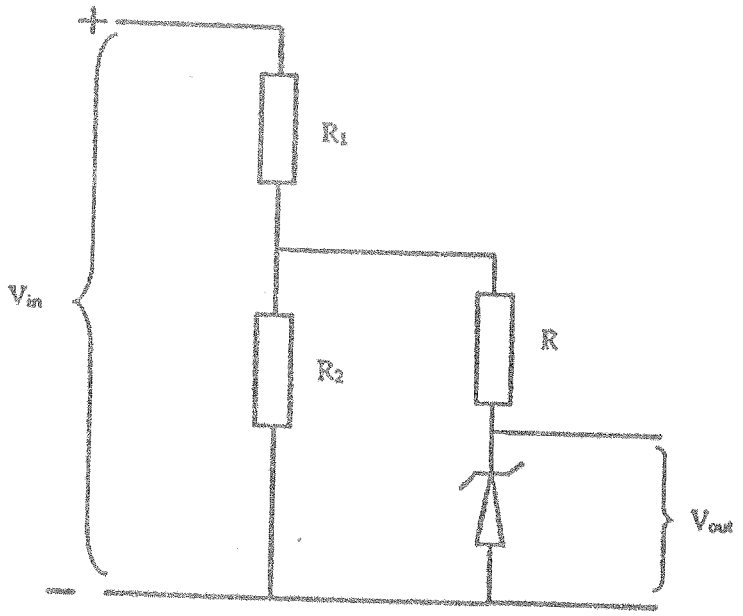
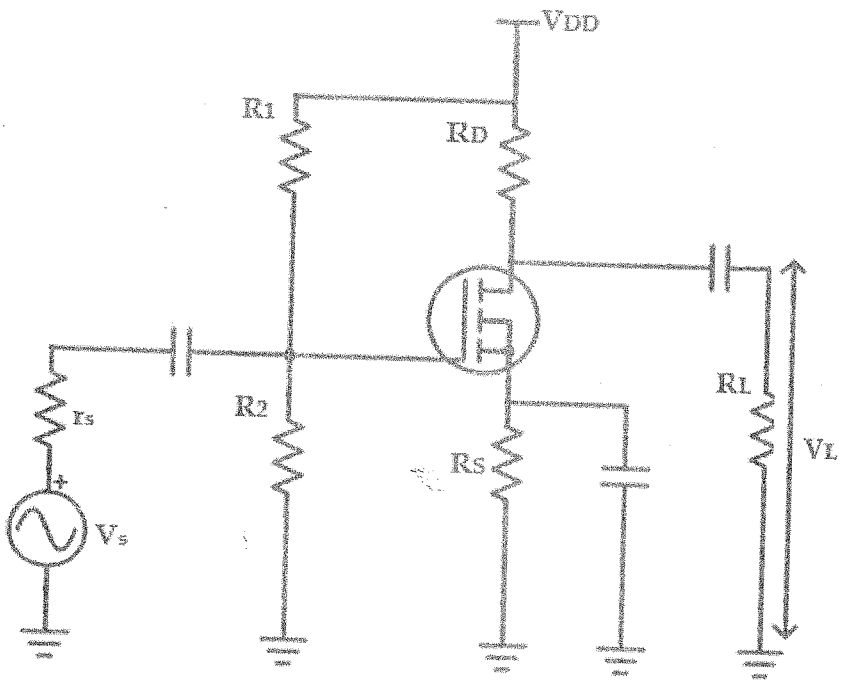


Figure Q3 (a)-A part of power supply unit



V_{DD}	= +18V
R_1	= 47 MΩ
R2	= 22 MΩ
R_D	= 2.2 kΩ
R_S	= 500 Ω
r_s	= 10 kΩ
R_L	= 100 KΩ

Figure Q3 (c)

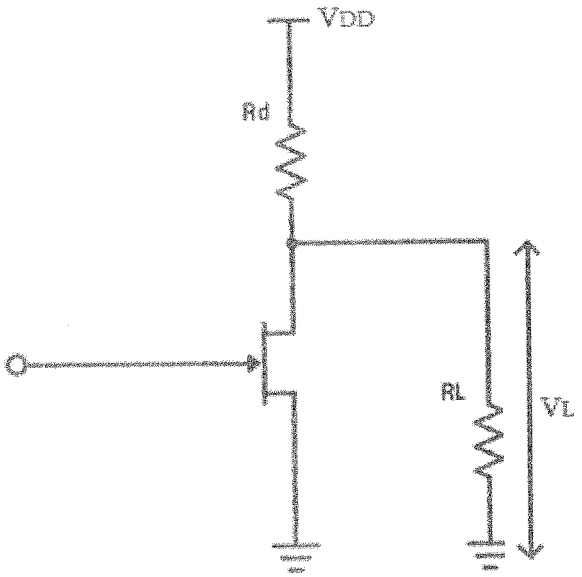


Figure Q4

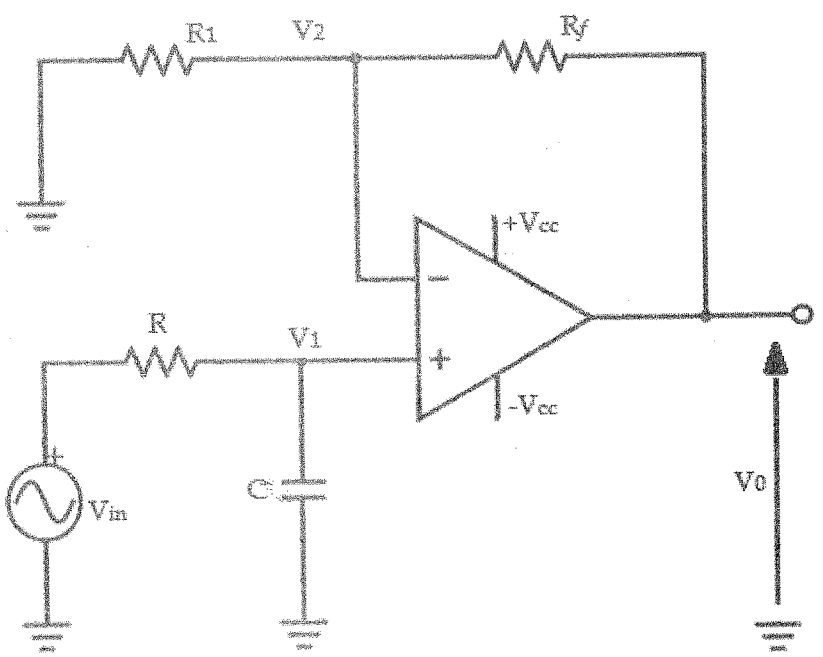


Figure Q2

```
module demux ( D, select, Q);
input[1:0]      D;
input   select;
output  Q;
wire            y0,y1;
assign  y0 = (~select) & D[0];
assign  y1 = y0  ^ D[1];
assign  Q = y0 | y1;
endmodule
```

Figure Q5 c) : Verilog code of a Test Module

```
module fsm_using_single_always (clock,reset,req_0,req_1,gnt_0,gnt_1);
 input   clock,reset,req_0,req_1;
 output  gnt_0,gnt_1;

 reg     gnt_0,gnt_1;

 parameter SIZE = 3;
 parameter IDLE  = 3'b110,GNT0 = 3'b101,GNT1 = 3'b011 ;
 reg   [SIZE-1:0]state;
 always @ (posedge clock)
 begin : FSM
 if (reset == 1'b1) begin
  state <= IDLE;
  gnt_0 <= 0;
  gnt_1 <= 0;
 end else
  case(state)
   IDLE : if (req_0 == 1'b1) begin
             state <= GNT0;
             gnt_0 <= 1;
            end else if (req_1 == 1'b1) begin
             gnt_1 <= 1;
             state <= GNT1;
            end else begin
             state <= IDLE;
            end
   GNT0 : if (req_0 == 1'b1) begin
             state <= GNT0;
            end else begin
             gnt_0 <= 0;
             state <= IDLE;
            end
   GNT1 : if (req_1 == 1'b1) begin
             state <= GNT1;
            end else begin
             gnt_1 <= 0;
             state <= IDLE;
            end
    default : state <=  IDLE;
  endcase
  end
endmodule
```

Figure Q5 e) : Verilog code module