UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5, Examination in Engineering, August 2015

Module No: EE5201 Module Name: Computer Architecture

[1 Hour and 45 minutes]

[Answer all questions. Each question carries 10 marks]

Part II

Q1. a) State three major architectural concepts of John von Neumann Machines. [1 Mark]

b) Draw the major components and their interconnection of John von Neumann architecture in a block diagram. Indicate, name and describe the function of all components and sub-components. [1 Mark]

c) What is logic and memory performance gap? What are the current technologies that aim to reduce the performance gap. Describe one of them. [2 Marks]

d) State Gordon Moore's Law. What are the consequences of this law? [2 Marks]

e) Give the memory hierarchy of modern computer systems based on their processing speed. [2 Marks]

f) Compare and contrast between SRAM and DRAM. Why SRAM is used in small amounts although the SRAM is faster than DRAM? [2 Marks]

Q2. a) State the Principle of Locality of Reference. [1 Mark]

b) Give a simple pseudo coding example, in which the locality of reference is clearly evident. [1 Mark]

c) What are the main Cache memory mapping functions. [2 Marks]

d) Indicate the meaning of Cache Memory mapping parameters; Word, Block, Line and Tag, in an appropriate diagram, to show their meanings. [2 Marks]

e) Consider the 16 MByte memory which is connected to the CPU through 64KBytes of Cache memory, having Blocks of size 4 Words. Size of a Word is 1 Byte.

i. Draw a block diagram of Cache and Main Memory indicating the direct mapping parameters; Word, Block, and Tag.

ii. What is the Tag, Line and Word for the Memory Read address 54 hex?

[2 Marks]

f) Mention the major drawback of Direct Mapping with respect to performance. [2Marks]

Q3. a) What is the purpose of the interrupt mechanism found in CPUs? [1 Mark]

b) In which point of the Instruction Cycle, is the Interrupt Sub-Cycle executed? You may use the state transition diagram to describe. [1 Mark]

c) Describe the major steps of interrupt execution of a CPU with respect to execution transfer, with the aid of a block diagram. [2 Marks]

d) Describe the purpose of Interrupt Vector Table found in Intel 8086 based systems? [2 Marks]

e) What are software interrupts? Give an example to illustrate its application. [2 Marks]

f) Intel 8086 processor machines usually consists of the Intel 8259 based hardware interface for I/O devices. Explain the basic functions that Intel 8259 based interface should perform to properly cooperate with Intel 8086 for correct implementation of external interrupts. For your explanation, use appropriate timing and block diagrams. [2 Marks].