UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 4 Examination in Engineering: November 2022

Module Number: EE4303 **Module Name: Digital Electronics**

[Three Hours]

[Answer **all questions**, each question carries 10 marks]

[Attach page 5 to your answer script]

Q1 a) Consider the Karnaugh Map (k-Map) given in Figure Q1.1

i) Name two groups that are Essential Prime Implicants.

ii) Name a group that is a Non-Essential Prime Implicant.

iii) Name a group that is a Non-Prime Implicant.

[2 Marks]

b) Figure Q1.2 shows the k-map of a Boolean function of five variables P, Q, R, S and X. What is the minimum sum-of-product (SOP) expression for the function?

[2 Marks]

c) Use a k-Map to generate a simple Boolean expression for the truth table shown in Table Q1.1 and draw a circuit using switches and a bulb to demonstrate the expression.

[2 Marks]

d) Simplify the following Boolean function, using Quine-McCluskey tabular method.

$$f(W,X,Y,Z)=\sum m(2,6,8,9,10,11,14,15)$$

[4 Marks]

Q2 a) Figure Q2.1 shows a sequential circuit with T flip flops. Show the state table and state diagram for the circuit in Figure Q2.1.

[2 Marks]

b) Determine the output states Q and $\overline{Q}$ for the J-K flip-flop in Figure Q2.2. (A), given the pulse inputs shown in Figure Q2.2 (B). Draw the output on page 5 and attach it to your answer script. Line 1 and line 2 are provided if you need for rough work, but only Q and $\overline{Q}$ will be evaluated.

[2Marks]

c) Consider circuit in Figure Q2.3; Explain what would happen if the upper AND gate's output were to become "stuck" in the high state regardless of its input conditions. What effect would this kind of failure have on the counter's operation?

[2 Marks]

d) A sensor boolean output is being monitored using a microprocessor system as shown in Figure 2.4 (A). However, the events detected by the sensor come and go much faster than the microprocessor can sample them (i.e. the pulses output by the sensor are too brief to be "caught" by the microprocessor every time). One solution for this is given in Q2.4 (B). Explain how this D-type flip-flop works to solve the problem, and what action the microprocessor has to take on the output pin to make the flip-flop function as a detector for multiple pulses.

[4 Marks]

Q3 a) State the excitation table for the RS latch given in Figure Q3.1.

[1 Mark]

b) Consider the asynchronous circuit given in Figure Q3.2 in which there are two inputs X1 and X2 and two outputs Y1 and Y2.

i) Derive Boolean functions for the inputs to NOR gates.

[1 Mark]

ii) Check the necessary condition that should be satisfied by inputs of the RS latch is satisfied.

[1 Mark]

iii) Derive the transition table using the result in part a). Clearly show the steps.

[4 Mark]

iv) Comment on the stability of the circuit giving reasons in point form.

[1 Mark]

v) Evaluate for Race conditions and list the types of identified Race conditions.

[1 Mark]

vi) Draw the flow table, state transition diagram and provide a new state assignment with avoids any Race conditions.

[1 Mark]

Q4 a) Answer the questions considering Table Q4.1 extracted from the datasheet of 74-Series TTL logic family.

i) Calculate the Figure of merit of a standard gate of the given logic family.

[1 Mark]

ii) Suppose that output from High-power TTL circuit feeds into multiple inputs of the same type and each of the inputs drops the voltage of the said output by 0.05 V. Identify the fan-out in this scenario.

[1 Mark]

iii) Suppose a circuit is operating in an environment with an additive noise centered at 0V and has a peak value of ±0.35 V. Recommend which of the families to be used in the circuit out of Low-power, High-power and Shottky TTL subfamilies.

[1 Mark]

b) Consider the logic circuit given in Figure Q4.1 in which Y is the output and A, B, C, and D are the inputs. Derive the logic equation for Y giving reasons.

[2 Marks]

c) Consider the logic circuit given in Figure Q4.2 in which A and B are the inputs and Vout is the output. The Base-Emitter voltage drop is 0.75 V.

i) State necessary assumptions and calculate the reference voltage V_R at the base of Q_R transistor.

[1 Mark]

ii) Calculate Vout given that A is set to -1.205 V and B is set to -1.435 V.

[1 Mark]

iii) Calculate Vout given that both A and B are set to -1.435 V.

[2 Mark]

iv) Identify the logic function of the output in terms of A and B, giving reasons.

[1 Mark]

Q5 a) Using only unit delay elements, multipliers and adders, sketch the signal flow graph of the filter with system function;

$$H(z^2) = \sum_{n=0}^{4} b_n z^{-2n}$$

[1 Mark]

b) Find the transfer function of the filter block diagram shown in Figure Q5.1.

[3 Marks]

c) Calculate the first four terms of the impulse response of a filter given by the following difference equation.

$$y[n] = x[n] + x[n-1] + \frac{1}{2}y[n-1]$$

[2 Marks]

d) Consider two students, namely, Student A and Student B. Student A implements an FIR filter for a certain application, while Student B implements an elliptic filter for the same application. Discuss the advantages and disadvantages of each of the chosen filter types. State your choice between the two? State the factors that would influence your decision?

[4 Marks]

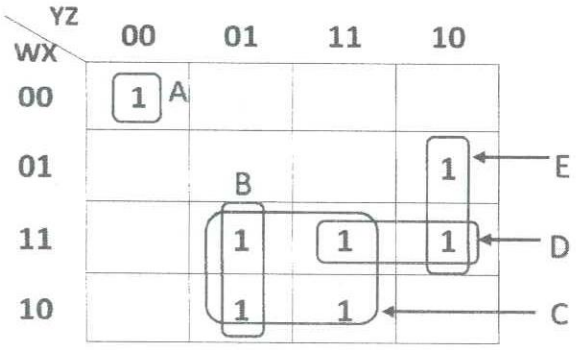

Figure Q1.1

RS \ PQ	00	01	11	10
00	0	0	0	0
01	1	0	0	1
11	1	0	0	1
10	0	0	0	0

X = 0

RS \ PQ	00	01	11	10
00	0	1	1	0
01	0	0	0	0
11	0	0	0	0
10	0	1	1	0

X = 1

Figure Q1.2

Table Q1.1

A	B	C	D	Output
0	0	0	0	**1**
0	0	0	1	**0**
0	0	1	0	**1**
0	0	1	1	**0**
0	1	0	0	**1**
0	1	0	1	**1**
0	1	1	0	**1**
0	1	1	1	**1**
1	0	0	0	**1**
1	0	0	1	**0**
1	0	1	0	**1**
1	0	1	1	**0**
1	1	0	0	**1**
1	1	0	1	**1**
1	1	1	0	**1**
1	1	1	1	**1**

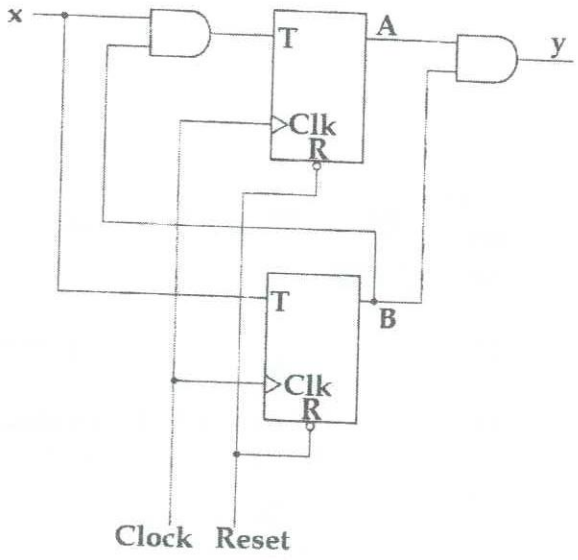

Figure Q2

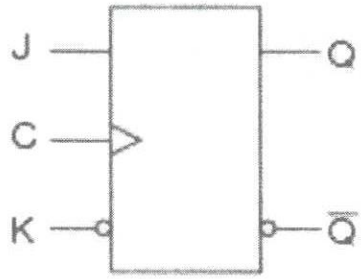

Figure Q2.2 (A)

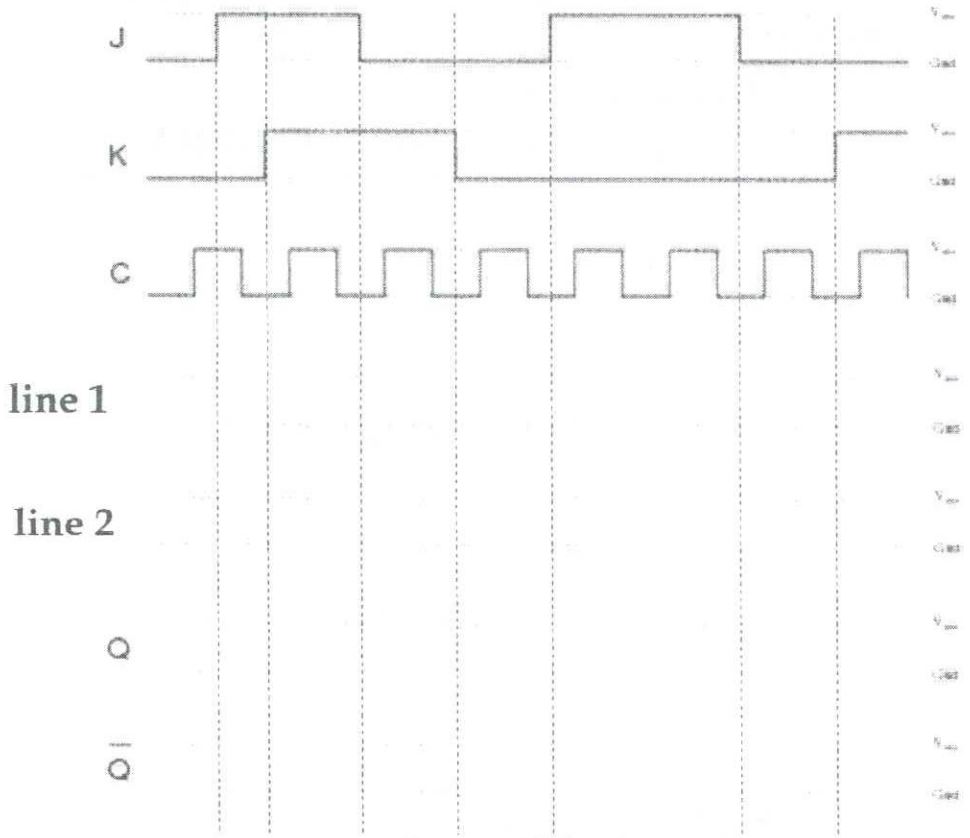

Figure Q2.2. (B)

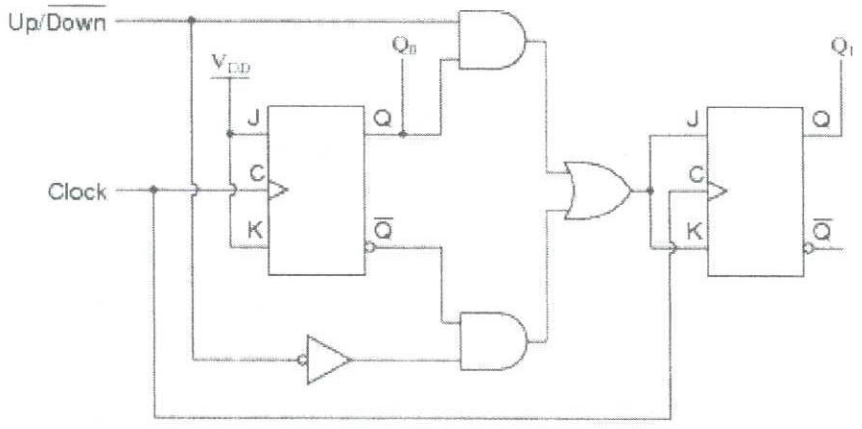

Figure Q2.3

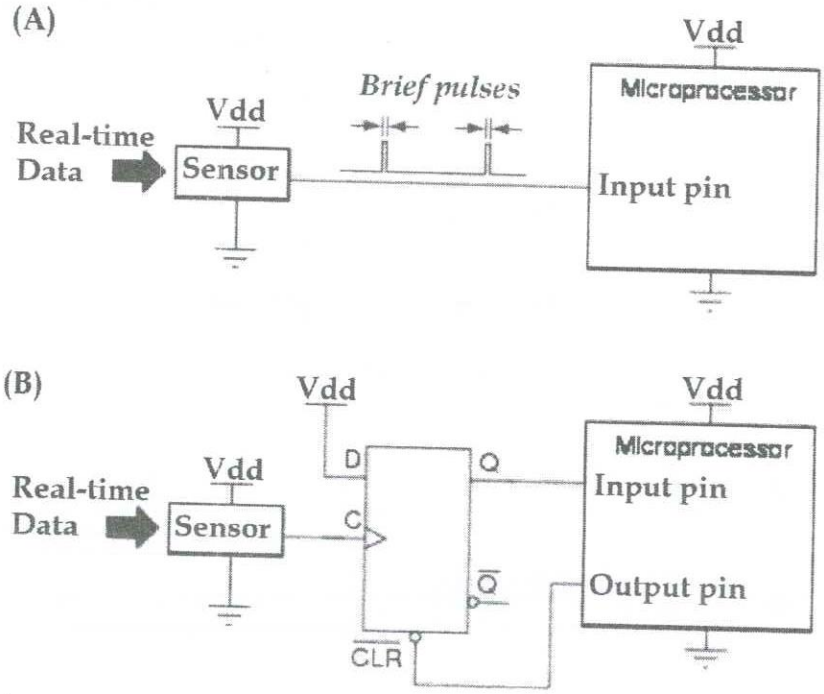

Figure Q2.4

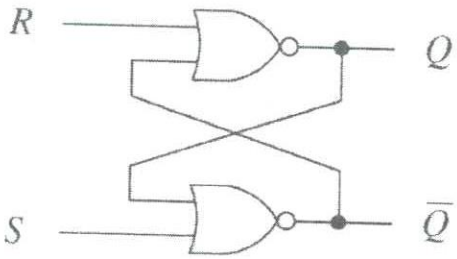

Figure Q3.1

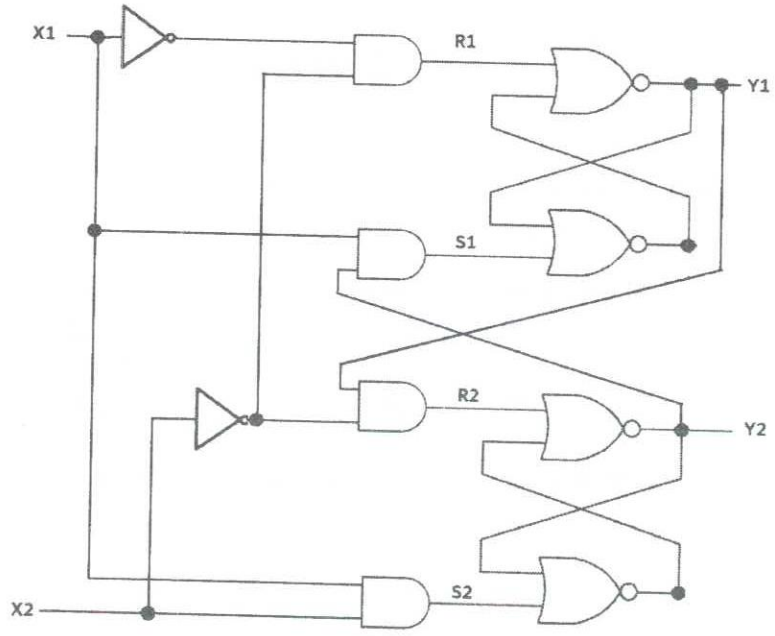

Figure Q3.2

Table 4.1

PARAMETERS	74-Series TTL Sub-families							UNITS
	Standard	L	H	S	LS	AS	ALS	
Propagation Delay (2-input NAND gate)	9nS	33	6	3	8	2	4	nS
Power Dissipation (per gate)	10 mW	1	22	20	2	22	1	mW
V_{IH}	2.0V	2.0	2.0	2.0	2.0	2.0	2.0	V
V_{OH}	2.4V	2.4	2.4	2.7	2.7	V_{DD}-2V	V_{DD}-2V	V
NM-H	400 mV	400	400	700	700	700	700	mV
V_{IL}	0.8V	0.7	0.8	0.8	0.8	0.8	0.8	V
V_{OL}	0.4V	0.3	0.4	0.5	0.5	0.5	0.5	V
NM-L	400 mV	300	400	300	300	300	300	mV

N = Standard TTL
L = Low-power TTL
H = High-power TTL
S = Schottky TTL
LS = Low-power Schottky
AS = Advanced Schottky
ALS = Advanced Low-power Schottky TTL
F = FAST TTL (Fairchild ALS TTL)
C = CMOS version of TTL device
HC = High-speed CMOS, with CMOS-compatible inputs
HCT = High-speed CMOS, with TTL-compatible inputs
AC = Advanced high-speed CMOS
ACT = Advanced high-speed CMOS with TTL-compatible inputs

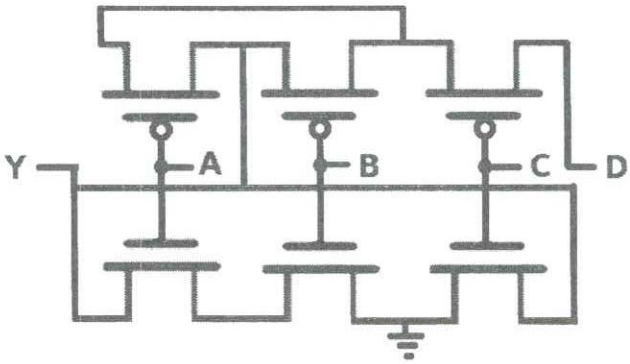

Figure Q4.1

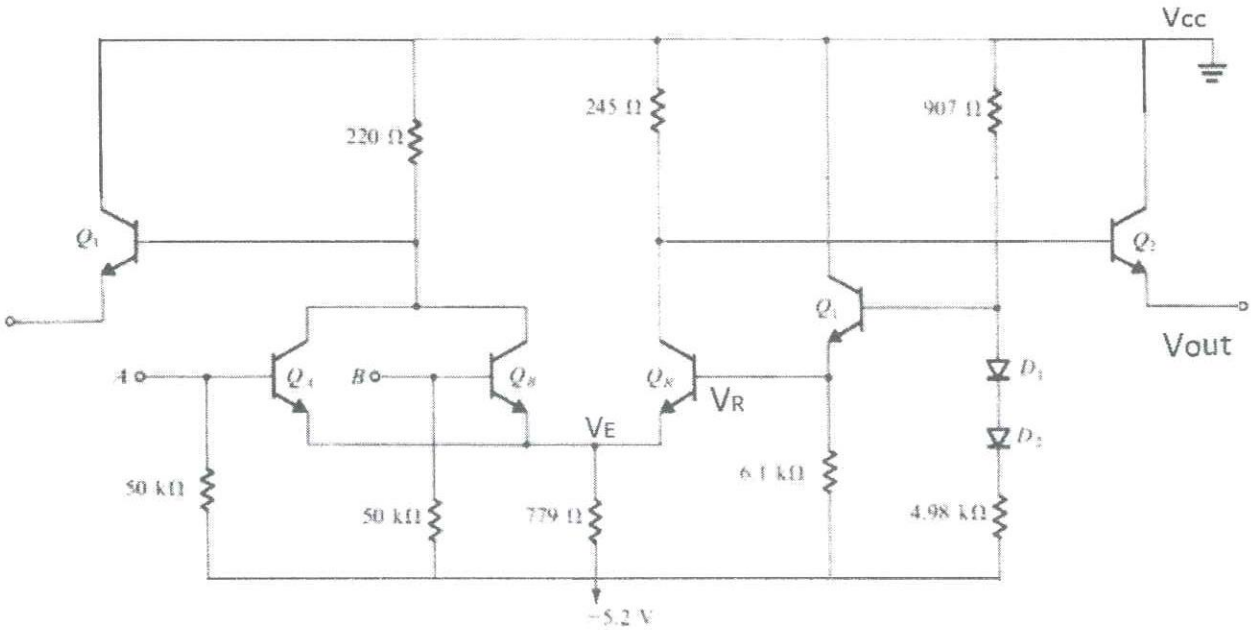

Figure Q4.2

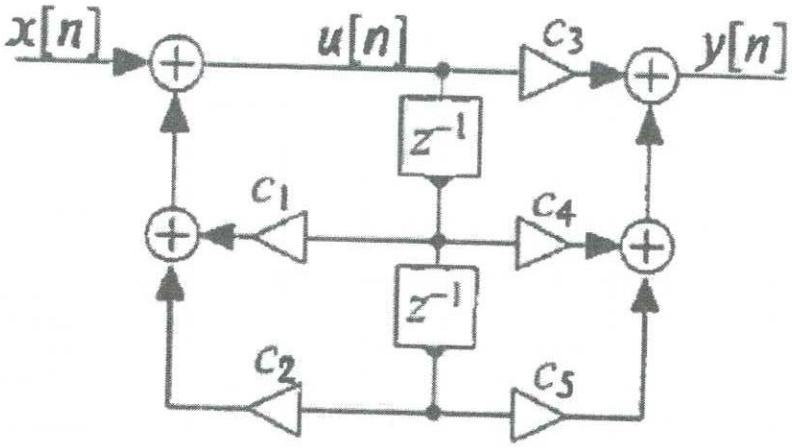

Figure Q5.1