UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 02 Examination in Engineering: February 2023

Module Number: EE2202   **Module Name: Introduction to Electronic Engineering**

[Three Hours]

[Answer all questions]

- Question paper consists of two parts. Part I: MCQs and Part II: Essay.
- **You should first answer the Part I on the provided answer sheet for MCQs (Page 12).**
- **Part I answer sheet for MCQs (Page 12) will be collected after 45 minutes.**

Part I: Multiple Choice Questions

- **Part I** of this question paper contains 25 MCQ questions. Time allocated is **45 minutes**.
- Answer all questions. Each question carries 0.5 Marks.
- Mark the answers on the provided **answer sheet for MCQs (Page 12)**.
- For each question, put **X** mark on the letter: a), b), c), or d) which corresponds to the correct answer, by using a black or blue ball-point pen.

Q1. 1) Identify the expressions which correctly states the distributive law of Boolean algebra.

    a) $x + y = y + x$ c) $x + y.z = (x + y).(x + z)$

    b) $\bar{\bar{x}} = x$ d) $(x \cdot y) \cdot z = x \cdot (y \cdot z) = x \cdot y \cdot z$

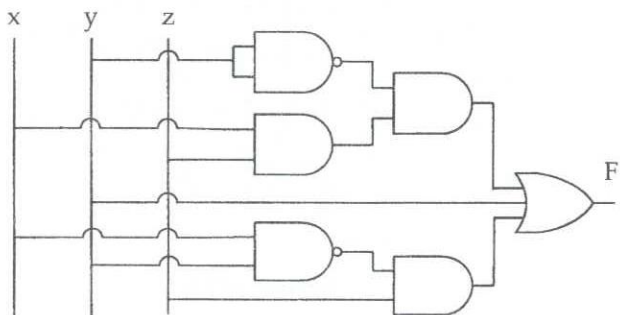2) Identify the expression which gives the minimized function (F) of the digital logic circuit given in Figure Q1.2.

Figure Q1.2

    a) $x + y$ c) $x + yz$

    b) $y + z$ d) $y\bar{z}$

3) Consider the SR Flip-Flop (FF) with only NOR gates given in Figure Q1.3. The FF has two useful states Q and Q' which are normally complemented with each other. Identify the statements which incorrectly explains the basic function of SR-FF.
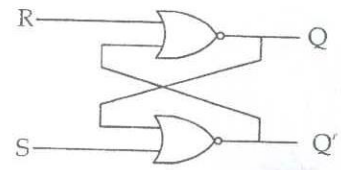

Figure Q1.3

a) Under normal conditions, both inputs of SR-FF remain at 0.

b) The application of momentary 1 to the S causes the state to be 1. (Q = 1)

c) When both inputs are at 0, the application of 1 to the R causes the state to be 1. (Q = 1)

d) If 1 is applied to both inputs of FF, the FF goes to an indeterminate state.

4) Identify the state which occurs in a JK flip-flop when both inputs J and K are 1.

a) Set state
b) Memory state
c) Reset state
d) Toggle state

5) Identify the inputs given to S and R when a clock enabled SR-FF is converted to JK-FF.

a) $K\overline{Q}$ and JQ, respectively
b) $J\overline{Q}$ and KQ, respectively
c) JQ and $K\overline{Q}$, respectively
d) KQ and $J\overline{Q}$, respectively

6) Identify the correct statement(s) related to the digital logic circuit consisting of a logic element P with inputs x, y, and z as given in Figure Q1.6.
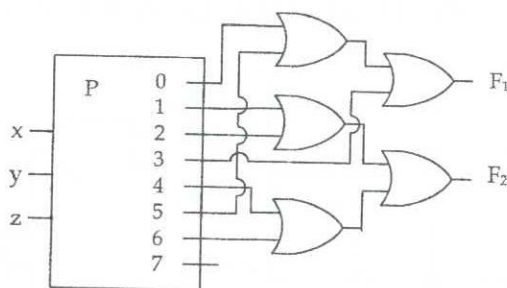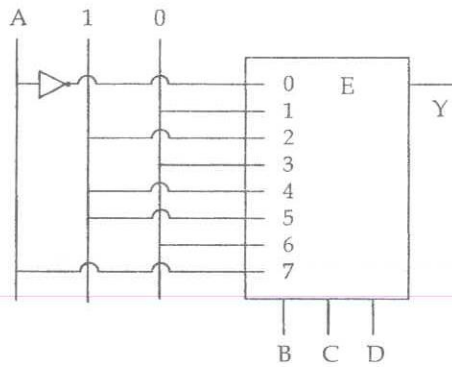

A. $F_1 = \Sigma m\,(1,4,6)$ and $F_2 = \Sigma m\,(2,3,5,7)$
B. Logic element P is a 3x8 Multiplexer.
C. $F_1 = \Sigma m\,(0,3,5)$ and $F_2 = \Sigma m\,(1,2,4,6)$
D. Logic element P is a 3x8 Decoder.
E. This is a sequential logic circuit.

Figure Q1.6

a) A, B and E only
b) C and D only
c) B, C and E only
d) A and D only

7) Identify the incorrect statement(s) related to the digital logic circuit consisting of a logic element E with inputs A, B, C, and D given in Figure Q1.7.

Figure Q1.7

P. $Y = \Sigma m\ (0,2,4,6,10,12,13,15)$
Q. Logic element E is a 3x8 Multiplexer.
R. This is a Combinational logic circuit.
S. Logic element E is an 8x1 Multiplexer.

a) P and Q only   c) P, Q and S only

b) R and S only   d) All

8) The input functions of the logic circuit illustrated in Figure Q1.8 (a) are expressed in eq. Q1.8(1) and Q1.8(2), respectively. Identify the states (Q) of the logic circuit when the inputs (x,Q) are **00** and **10**, respectively.
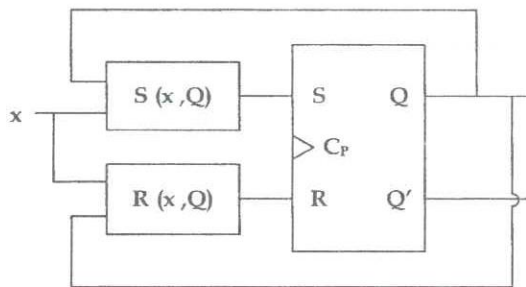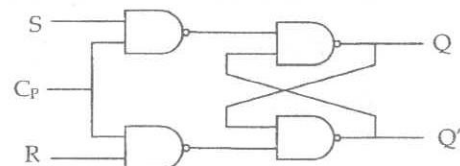

Figure Q1.8(a)

Figure Q1.8(b)

$S(x, Q) = \Sigma m\ (0, 3) - Q1.8(1)$ and $R(x, Q) = \Sigma m\ (1, 3) - Q1.8(2)$

a) **00**   c) **01**

b) **10**   d) **11**

9) Identify the flip-flop given in Figure Q1.9.
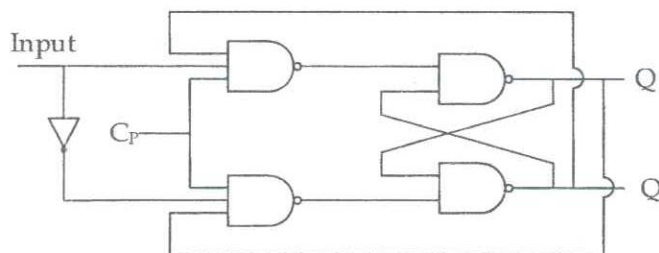

Figure Q1.9

a) SR – Flip-Flop   c) JK – Flip-Flop

b) D – Flip-Flop   d) T – Flip-Flop

10) Identify the <u>correct</u> statement(s) related to the triggering of flip-flops (FFs).

     A. The state of an FF is switched by change in the control clock pulse.
     B. The state transition of an FF starts as soon as the clock pulse changes to **1**.
     C. The new state of an FF remains at the output as long as the pulse is active.
     D. For edge triggered FFs, any changes in data input will change the state as long as the pulse is active.

a) A and B only   c) A and C only

b) B, C and D only   d) All

From question 11 to 13, identify the answer containing the most suitable words/phrases to fill in the blanks.

11) Drift current is due to _____

a) Variation in carrier concentration

b) The applied electric field over a given distance

c) Random motion of electrons

d) Recombination of holes and electrons

12) Diffusion current is due to _____

a) The applied electric field over a given distance

b) Variation in carrier concentration

c) Random motion of holes

d) Recombination of holes and electrons

13) A p-type semiconductor material is doped with _____ impurities.
An n-type semiconductor material is doped with _____ impurities.

a) acceptor, donor   c) donor, donor

b) acceptor, acceptor   d) donor, acceptor

14) When physical contact between a p-region & n-region is established, which of the following is most likely to take place?

a) Electrons from the n-region diffuse to p-region

b) Holes from the p-region diffuse to n-region

c) Both above-mentioned statements are true

d) Nothing will happen

15) Identify the correct statement regarding an unbiased p-n junction diode.
   a) Diffusion does not take place
   b) Diffusion of electrons & holes goes on infinitely
   c) There is zero electrical potential across the junctions
   d) Charges establish an electric field across the junctions

16) Identify the phenomenon evaluated by the equation $J_n=qn\mu_nE$ (A/cm^2).
   a) Drift current
   c) Diffusion current
   b) Drift current density
   d) Diffusion current density

In questions 17 – 21, N_A, N_D, and n_i has their usual meaning while $n_i = 10^{10}$ cm^{-3}.

17) A p-n silicon junction has uniform doping levels of $N_A = 2 \times 10^{16}$ cm^{-3} and $N_D = 3 \times 10^{18}$ cm^{-3}. Determine the hole concentration of the p-region.
   a) 3×10^{18} cm^{-3}
   c) 10^{10} cm^{-3}
   b) 2×10^{16} cm^{-3}
   d) 5000 cm^{-3}

18) A p-n silicon junction has uniform doping levels of $N_A = 2 \times 10^{18}$ cm^{-3} and $N_D = 3 \times 10^{16}$ cm^{-3}. Determine the electron concentration of the n-region.
   a) 2×10^{18} cm^{-3}
   c) 10^{10} cm^{-3}
   b) 3×10^{16} cm^{-3}.
   d) 5000 cm^{-3}

19) A p-n silicon junction has uniform doping levels of $N_A = 2 \times 10^{16}$ cm^{-3} and $N_D = 3 \times 10^{16}$ cm^{-3}. Determine the electron concentration of the p-region.
   a) 2×10^{16} cm^{-3}
   c) 10^{10} cm^{-3}
   b) 3×10^{16} cm^{-3}
   d) 5000 cm^{-3}

20) A p-n silicon junction has uniform doping levels of $N_A = 3 \times 10^{18}$ cm^{-3} and $N_D = 2 \times 10^{16}$ cm^{-3}. Determine the hole concentration of the n-region.
   a) 3×10^{18} cm^{-3}
   c) 10^{10} cm^{-3}
   b) 2×10^{16} cm^{-3}
   d) 5000 cm^{-3}

From question 21 to 22, identify the answer containing the most suitable words/phrases to fill in the blanks.

21) A FET is a_____ controlled device.
    A BJT is a_____ controlled device.

    a) Current, Voltage   c) Current, Current

    b) Voltage, Voltage   d) Voltage, Current

22) Whenever a JFET operates above pinch-off voltage _____

    a) Drain current starts decreasing

    b) Drain current increases steeply

    c) Depletion regions become smaller

    d) Drain current remains nearly constant

23) Identify the correct statement regarding the biasedness of the gate-source junction of a properly functioning JFET.

    a) It is unbiased   c) It is forward biased

    b) It is reverse biased   d) None of the above

24) Identify the reason for N-channel MOSFETs is preferred than a P-channel MOSFET.

    a) It is cheaper   c) It has better drive capability

    b) It is faster   d) It has better noise immunity

25) Identify the most commonly used insulating layer material for MOSFET.

    a) GeO_2 c) As_2O_5

    b) Al_2O_3 d) SiO_2

PART II - Essay Questions

Answer all questions. Each question carries 12.5 Marks.

Q2   a)   i)   Plot the input/output characteristic curves of the circuits depicted in Figure Q2(a) using the **ideal diode model**. Assume $V_B = 2$ V.

   ii)   Plot the input/output characteristics of the circuits depicted in Figure Q2(a) using the **constant voltage diode model** for the diodes. Assume $V_B = 2$ V, $V_{D,on} = 700$ mv.

(I)   (II)   (III)

(IV)   (V)
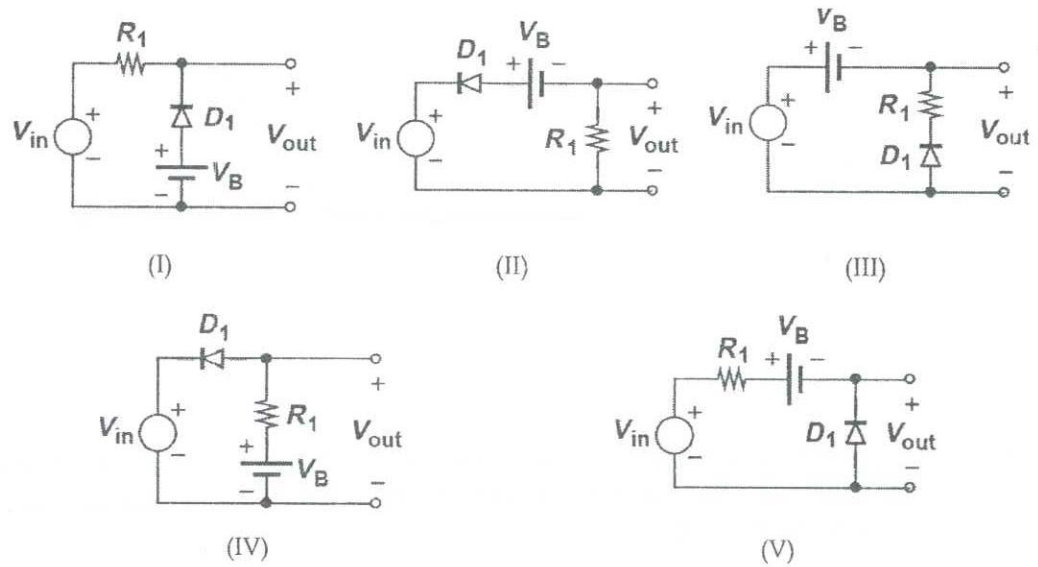
Figure Q2(a)

[7.5 Marks]

b)   Figure Q2(b) shows a Si diode circuit to add a dc level to an input signal v_S which has an average value of zero. The input signal (v_S) is a square wave alternate between 10V and -10V. The period of the square wave is T. Value of the resister R_L is equal to R_1.

   i)   Plot the output voltage (v_L) over time (t), considering the constant voltage model for the diode $V_{D,on} = 700$ mv.

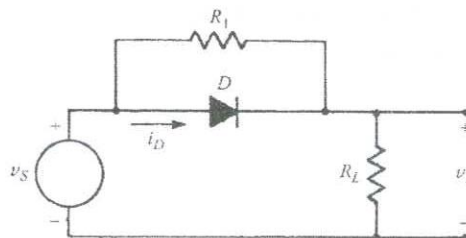   ii)   Evaluate the average value of the output signal.

Figure Q2(b)

[3.0 Marks]

c) Figure Q2(c) shows the function ReLU (Rectified Linear Unit), which is used as an activation function in artificial neural networks. Propose a diode circuit to perform the ReLU function to a given input voltage, assuming that the diode is ideal.
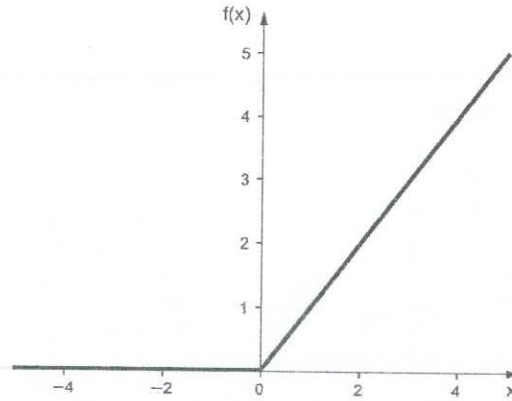

Figure Q2(c)

[2.0 Marks]

Q3 a) The emitter current in an NPN transistor is 8.4 mA. If 0.8% of the minority carriers injected into the base recombine with holes and the leakage current is 0.1 µA, determine the following.

   i)   The base current.

   ii)   The collector current.

   iii) The exact value of α.

   iv)   An approximate value of α, neglecting I_{CBO}.

[2.5 Marks]

   b) i)   Sketch the output characteristics for an NPN Si transistor in common-emitter configuration and saturation, active and cut-off regions.

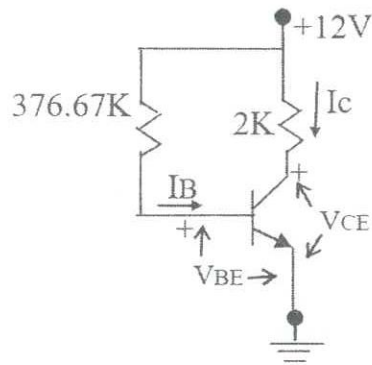   ii) The Si transistor in the C-E bias circuit shown in Figure Q3(b) has a β of 100. Find the bias point.

Figure Q3(b)

[3.5 Marks]

c) Figure Q3(c) shows a biased circuit with resisters for an NPN Si transistor in common base configuration.

   i)   Derive an expression for the load line.

   ii) Find the resistance R_C and R_E, when $V_{CB} = 4V$, $I_C = 3$ mA, $V_{CC} = -V_{EE} = 10V$, $V_{BE} = 0.7$ V, and $\beta = 120$.
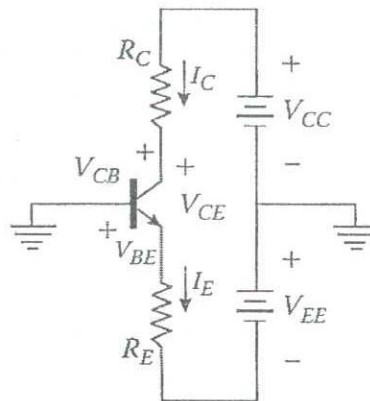

Figure Q3(c)

[3.5 Marks]

d) Sketch the internal structure of an N-Type Enhancement MOSFET, name the terminals, and briefly explain the mechanism behind the formation of the N-channel in a biased E-MOSFET.

[3.0 Marks]

Q4 a) i) Compare and contrast the basic function of combinational and sequential logic circuits.

   ii) Briefly describe the operation of a decoder and a multiplexer.

   iii) Write the characteristic table of a clock enabled SR flip-flop (FF).

[2.5 Marks]

b) You are required to construct a digital logic circuit whose output function is expressed in (Q4.1).

$$F(A, B, C, D) = \sum m(2, 3, 4, 5, 6, 10, 11, 12, 13, 14, 15) - (Q4.1)$$

i)   Derive the truth table of the required digital logic circuit.

ii) Design the required logic circuit using a minimum number of NAND gates.

iii) Design the required logic circuit using a 4x16 decoder and OR gates having two or three inputs.

iv) Design the required logic circuit with a 4x1 multiplexer and any other necessary logic gates.

[5.5 Marks]

c) You are required to analyze the digital logic circuit given in Figure Q4(c)-I, which consists of a positive edge triggered, clocked LM-FF.
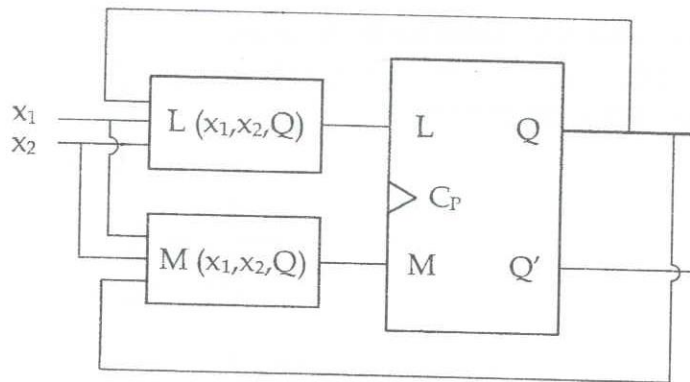

Figure Q4(c)-I

The LM-FF has two inputs **L** and **M** and they operate as follows.

- If **LM** = 00, the next state of the FF output is 0.
- If **LM** = 01, the next state of the FF output is the same as present.
- If **LM** = 10, the next state of the FF output is the complement of present.
- If **LM** = 11, the next state of the FF output is 1.

i)   Derive the characteristic table of the LM-FF.

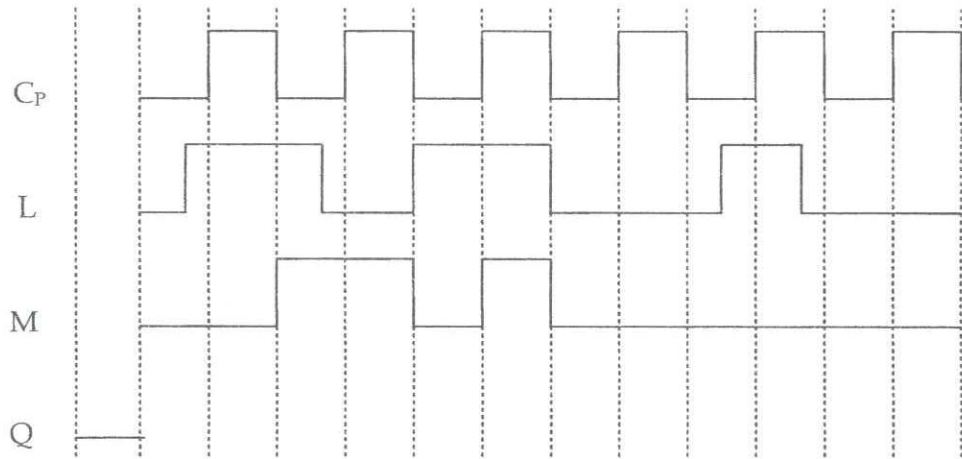ii) Determine the output waveform (Q) of the LM-FF for the clock C_P and input signals given in Figure Q4(c)-II.

Figure Q4(c)-II

iii) Derive the state table of the circuit given in Figure Q4(c)-I for the given input functions in $(Q4.2)$ and $(Q4.3)$.

$$L(x_1, x_2, Q) = \overline{(x_1 + Q + \overline{x_2})}(\overline{Q} + \overline{x_2}) \qquad - (Q4.2)$$
$$M(x_1, x_2, Q) = \sum m(0, 2, 3, 4, 5, 6) \qquad - (Q4.3)$$

Hint: Use the following headings in your state table of the logic circuit.

x_1	x_2	Q_n	L	M	Q_{n+1}	$\overline{Q_{n+1}}$

[4.5 Marks]