UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 2 Examination in Engineering: March 2014

Module Number: EE2202 **Module Name: Introduction to Electronic Engineering**

[Three Hours]

[Answer **all questions**, each question carries 10 marks]

All notations have their usual meanings

Q1 a) i. Sketch the bias circuit for an NPN transistor in Common-Base configuration that have DC sources V_{EE} and V_{CC} and currents I_E, I_B and I_C.

ii. What is the equation relating the currents?

iii. If the reverse saturation current is I_{CBO} and the Common-Base DC current gain is α, show that $Ic \approx \alpha I_E$.

[2 Marks]

b) i. Sketch the bias circuit for an NPN transistor in Common-Emitter configuration that has a single DC supply +Vcc and bias resistors R_B and R_C.

ii. Show that the Common-Emitter DC current gain $\beta = I_C / I_B$, where I_C and I_B are the collector and base currents respectively.

iii. Sketch the input and output characteristics for this circuit clearly labeling the axes and show the three operating regions in the output characteristics.

iv. Which two regions are utilized when the transistor is operating as a switch?

v. Derive an approximate value for the Base-Emitter voltage V_{BE}.

vi. Design the Common Emitter bias circuit for an NPN Si transistor with $\beta = 110$, that has a +15 V supply and a bias point current $I_C = 2.66$ mA and a voltage $V_{CE} = 7$ V.

[5.5 Marks]

c) i. Explain why we set a bias point in a transistor amplifier.

ii. What will happen if the bias point is set too high?

iii. What will happen if the output amplitude is too high?

iv. Give two actions which you can take to remove the effect in part iii.

v. What term describes these effects in parts ii) and iii)?

[2.5 Marks]

Q2 a) Figure Q2 a) shows a representative circuit of an amplifier connected to a source and a load. The voltage and current gains of the amplifier are A_v and A_i respectively. Give the equations for the overall voltage gain v_L/v_s and overall current gain i_L/i_s.

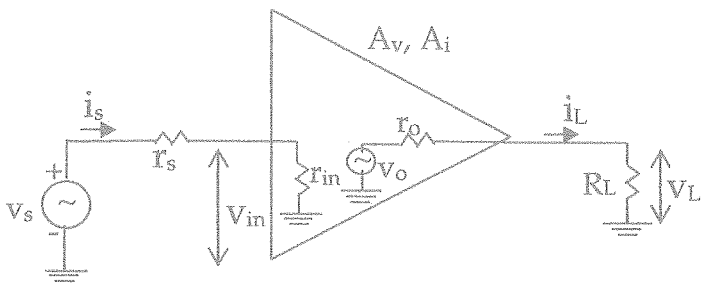


Figure Q2 a). [1 Mark]

b) i. Figure Q2 b) shows the AC voltages and currents for an NPN transistor in Common-Base configuration. The input emitter resistance is r_e and the output resistance is r_c respectively. What is the AC equivalent circuit for this transistor?

ii. Sketch the DC Common-Base amplifier circuit with a source of voltage v_s, and using its AC equivalent circuit. Then show that the voltage gain and current gain for the amplifier is $A_v = R_c/r_e$ and $A_i = \alpha$ respectively.

[3 Marks]

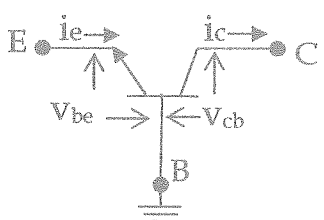


Figure Q2 b).

c) i. Figure Q2 c) shows the voltages and currents for an NPN transistor in Common-Emitter configuration where the emitter resistance r_e is drawn inside the transistor to show it is an internal parameter. Show that the input resistance to the transistor is $r_{in} = \beta\, r_e$ where β is the Common-Emitter DC current gain.

ii. Given that the output resistance is r_c/β where r_c is given by b) ii), draw the AC equivalent circuit of the transistor in Common-Emitter configuration.

iii. Give the DC circuit and its AC equivalent for an NPN Common-Emitter amplifier that has a voltage source v_s, and show that the voltage gain and the current gain for the amplifier is given by $A_v = -R_c/r_e$ and $A_i = \beta$ respectively.

iv. Why is the Common-Emitter amplifier a better voltage amplifier than the Common-Base amplifier?

[6 Marks]

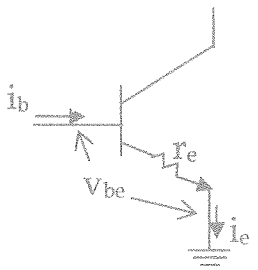


Figure Q2 c).

Q3 a) i. Sketch the structure of an N-Channel JFET and show the bias arrangement for DC sources V_{GS} and V_{DS} where G, D and S denotes the gate, drain and source terminals respectively.

ii. In the same figure, sketch the formation of the depletion regions for the two cases

I. $V_{DS} = 0$ in solid lines and

II. $V_{DS} \neq 0$ in dashed lines [1 Mark]

b) Figure Q3 b) shows the Drain-Source characteristics of a JFET?

i. What is the pinch-off voltage of the JFET?

ii. Calculate the saturation currents when $V_{GS} = -1$ V and $V_{GS} = -2$ V.

Hint: The equation giving the saturation current with the usual notations is

$$I_{D(sat)} = I_{DSS}\{ V_{DS(sat)}/V_p\}^2$$

iii. Derive the transfer characteristics of the JFET when $V_{DS} = 8$ V.

[2.5 Marks]

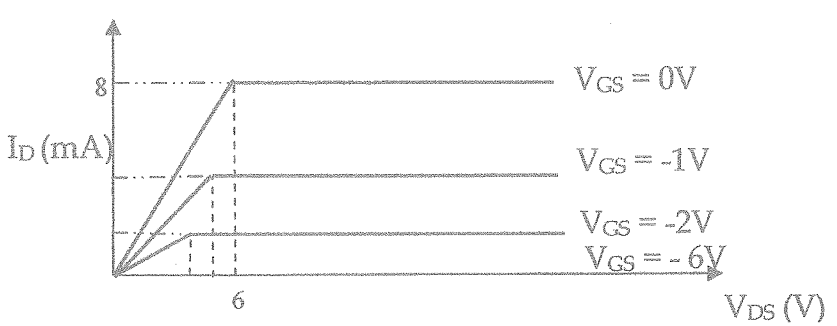


Figure Q3 b).

c) i. Use a sketch to illustrate the structure of an N-channel depletion type MOSFET.

ii. Briefly explain the operation of a depletion type N-channel MOSFET

[1.5 Marks]

d) What is meant by a sequential logic circuit? [0.5 Marks]

e) You are required to design a 2-bit binary counter (0 - 3) using D Flip-Flops to implement the circuit.

i. Complete the following state transition table

Present State		Next State		Flip Flop Input	
$Q_1(n)$	$Q_0(n)$	$Q_1(n+1)$	$Q_0(n+1)$	$D_1(n)$	$D_0(n)$
0	0	0	1		
0	1				
1	0				
1	1	0	0		

ii. Obtain the Boolean expressions for D_0 and D_1 inputs of the two D Flip Flops.

iii. Draw the complete circuit diagram to implement the 2-bit binary counter. You may use block diagram to represent the D Flip Flop. [4.5 Marks]

Q4 a) What is meant by a combinational logic circuit? [0.5 Marks]

b) Find the Boolean expression for the following circuit in Figure Q4 b). [1 Mark]

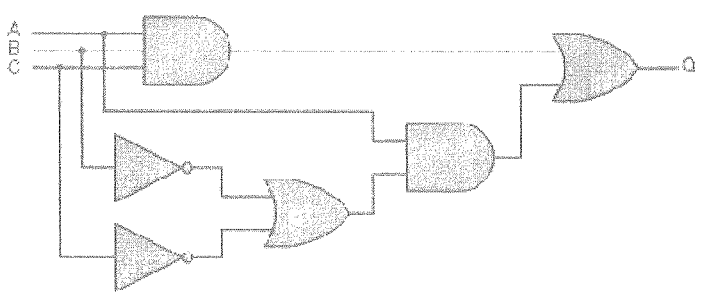


Figure Q4 b).

c) Find the Binary Coded Decimal (BCD) representation of the following decimal numbers.

i. 453_{10}

ii. 239631_{10} [1 Mark]

d) Find the 2's complement of the following, giving necessary calculations. You are required to use an eight (8) bit system.

i. $31_{10} - 32_{10}$

ii. $-50_{10} + 65_{10}$

iii. $-21_{10} - 32_{10}$ [3 Marks]

e) Using Boolean algebra, show that

i. $B.(A + C) + C = A.B + C$

ii. $[(A.B) + (A.B') + (A'.B')]' = A'.B$

iii. $(A'.B.C')'.(A.B'.C')' = C + [(A'.B') + (B.A)]$

Note: Give the steps of each derivation and state which axioms you use at each step.

[4.5 Marks]

Q5 You are required to design an N-bit full adder circuit and an N- bit subtract circuit using 2's complement method. You may use the following steps to implement the circuits.

- Design a 1-bit full adder circuit.
- Implement the N-bit full adder using the 1-bit full adder
- Implement the N-bit subtract circuit, modifying the N-bit full adder

a) i. Draw a truth table for the 1-bit full adder circuit.

Hint: $A_{in} + B_{in} + C_{in} = Carry_{out} + S_{out}$

$Carry_{out}$
C_{in}
A_{in}
B_{in} +
S_{out}

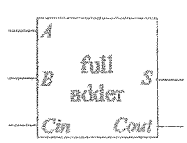
example : $1 + 1 + 1 = [(S_{out} = 1) + (Carry_{out} = 1)]$

ii. Populate the Karnaugh maps for $Carry_{out}$ and S_{out} using the truth table obtained in part i).

iii. Find the minimized Sum of Products (SOP) expression.

iv. Draw the circuit diagram of the 1-bit full adder circuit. [4 Marks]

b) i. Draw the N-bit full adder circuit using the 1-bit full adder obtained in part a). You may use the following logic symbol as the 1-bit full adder.



Hint:

$C_{out(N-2)} = C_{in(N-1)}$		$C_{out1} = C_{in2}$	$C_{out0} = C_{in1}$		
A_{N-1}	.....	A_2	A_1	A_0	
B_{N-1}	.....	B_2	B_1	B_0	+
S_{N-1}	.....	S_2	S_1	S_0	

ii. Determine the value of C_{in} in 0^{th} 1-bit full adder (C_{in0}) to implement the N-bit full adder circuit.

[3 Marks]

c) i. Draw the N-bit subtract circuit. You are required to modify the N- bit full adder circuit obtained in part b) to implement the N bit subtract circuit.

Hint :

Negative number representation: First invert all the binary bits and add 1.

A_{N-1}	.....	A_2	A_1	A_0			A_{N-1}	.....	A_2	A_1	A_0
B_{N-1}	.....	B_2	B_1	B_0	-	=	B_{N-1}'	.....	B_2'	B_1'	B_0'
S_{N-1}	.....	S_2	S_1	S_0						1	+
							S_{N-1}	.....	S_2	S_1	S_0

ii. Determine the value of C_{in} in 0^{th} 1-bit full adder (C_{in0}) to implement the N bit subtract circuit.

[3 Marks]