UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 4 Examination in Engineering: January 2022

Module Number: EE4303 **Module Name: Digital Electronics**

[Three Hours]

[Answer all questions, each question carries 10 marks]

Q1 a) Boolean expression for the output F of a combinational logic circuit is given by $F(A,B,C) = A + B'C$

i) State a unique feature of a combinational logic circuit.

ii) Express the function F as;

- a sum of minterms and
- a product of maxterms.

iii) Implement the function F assuming that you have **only** three two-input NAND gates and one two-input OR gate.

[4.0 Marks]

b) The control system of a power plant receives the following digital signals.

- Generator status G (G=1 if the generator is online, G = 0 if the generator is offline)
- Fuel level L (L= 1 if the tank's fuel level is acceptable, L = 0 if the tank's fuel level is low)
- Fuel tank temperature controller status C (C = 1 if the temperature controller is ON, C = 0 if the controller is OFF)
- Fuel temperature T (T= 1 if fuel temperature is acceptable, T = 0 if fuel temperature is low)

When the generator is offline, the fuel tank temperature controller should maintain tank's fuel temperature within acceptable limits.

Your task is to design a combinational logic circuit that could trigger a Fault F in the control system.

Fault signal F should be 1;

- if the generator is online and the tank's fuel level is low **OR**
- if the generator is offline and the fuel level is acceptable and the temperature controller is OFF **OR**
- if the generator is offline and the fuel level is acceptable and the temperature controller is ON and fuel temperature is low.

Fault signal F should be 0 in all the other circumstances.

i) Derive a truth table summarizing the given problem statement.

ii) Obtain a Boolean expression for F as a sum of minterms.

iii) Simplify the Boolean expression for F using Karnaugh Map Method.

iv) State an advantage and a drawback of Quine-McCluskey Algorithm compared to Karnaugh Map Method.

v) Implement your design using logic gates.

[6.0 marks]

Q2 a) You are given a novel clocked Flip-Flop (FF) named UV FF. A UV FF has two inputs U, V and an output Q. The characteristic table for a UV FF is given in Table Q2-a)

i) State two differences between a combinational logic circuit and a sequential logic circuit.

ii) Derive the excitation table for a UV FF.

[2.0 Marks]

b) State table for a sequence detector is given in Table Q2-b)
The detector circuit has one input named x. Its output y must be '1' when the intended sequence is detected and '0' otherwise. This sequence detector has to be implemented as a synchronous sequential logic circuit.

i) Obtain the state diagram considering the state table.

ii) Identify the sequence of inputs that will be identified by the sequence detector.

iii) Using "binary ascending" assignment technique, derive the binary coded state table. (The table should contain columns that indicate the following: Present state, Input, Next state, Output, FF input.)
Note: Use D FFs in your design.

iv) Obtain FF input equations and the output function in terms of present states and input.

v) Simplify the expressions obtained in part b) iv).

vi) Implement the sequence detector using FFs and logic gates.

[6.0 marks]

c) i) Stating reasons, classify the designed sequence detector into either Mealy model or Moore model.

ii) Considering the binary coded state table you developed in part b) iii), obtain the modified FF input column if you have to design the sequence detector using UV FFs.

[2.0 Marks]

Q3 a) i) State two differences between a synchronous sequential logic circuit and an asynchronous sequential logic (ASL) circuit.

ii) Briefly explain the fundamental mode of operation of an ASL circuit.

iii) Consider the flow table given in Figure Q3-a). Assign binary values to outputs at unstable states (denoted by "-") so that there are no momentary false outputs when the circuit switches between states.

[4.0 Marks]

b) An ASL circuit has two internal states and one output. It has two inputs (x_1, x_2). The two excitation functions (Y_1, Y_2) and the output function (z) that describe the circuit are given below.

$Y_1 = x_1x_2 + x_1y_2'$

$Y_2 = x_1 + x_1y_1y_2 + x_2y_1$

$z = x_1 + y_1 + y_2$

i) Obtain the circuit diagram using logic gates.

ii) Derive the transition table and the output map. Circle the stable states in the transition table.

iii) Comment with reasons, whether the circuit may become unstable for some input conditions.

[3.5 marks]

c) Consider the flow table given in Figure Q3-c).

i) Obtain the transition diagram for this flow table.

ii) Hence, show that it is not possible to make a race-free binary variable assignment for the states in the flow table by using only three states.

iii) Obtain the modified flow table with an appropriate race-free binary variable assignment for the states. Indicate your binary variable assignment for states in a transition diagram.

[2.5 marks]

Q4 a) The basic logic gate in most of the digital logic families is either a NAND gate or a NOR gate.

i) Show that NOT, AND, OR and NOR gates can be implemented by using only NAND gates.

ii) State the meanings of the acronyms RTL, DTL and TTL used to specify digital logic families.

iii) Explain the term *noise margin* of a logic gate.

[2.0 marks]

b) A design of a digital logic circuit consists of 44 two-input NAND gates and 51 two-input NOR gates. The circuit has to be implemented using TTL quadruple two-input NAND gate ICs and TTL quadruple two-input NOR gate ICs.

A quadruple IC contains four gates. For example, the schematic diagram of a TTL quadruple two-input NAND gate IC is shown in Figure Q4)-b). Specifications of the logic gates are given in Table Q4-b).

i) Calculate the noise margins of the gates used in this design.

ii) Calculate the fan-out of a NAND gate.

iii) Explain the importance of calculating the fan-out of logic gates in designing a digital logic circuit.

iv) Calculate the average power dissipation of a NAND gate and a NOR gate.

v) Stating any assumptions you make, estimate the minimum power rating of a suitable power supply for this circuit.

[6.0 marks]

c) Circuit diagram of the basic logic device in RTL logic family is given in Figure Q4-c).

i) Briefly explain the operation of this circuit and identify the implemented logic gate.

[2.0 marks]

Q5 a) Answer following questions regarding digital filters.

i) Describe the difference between 'sampling' and 'quantization'.

ii) Define a Discrete Time Signal.

iii) Describe how to avoid aliasing.

[2.0 marks]

b) Answer the following sections based on a 3 point moving average FIR filter
   i) Write the difference equation of the above filter and the block diagram.
   ii) Write down the transfer function of the above filter.
   iii) What are the poles and zeros of the above filter?

[3.0 marks]

c) The zeros of a certain filter are at 0.5 and poles are at $-0.6 \pm 0.3i$. Write the transfer function of this filter in the simplest form.

[2.0 marks]

d) Output sequence of a FIR filter is [1,0,0,2,0,1] in response to a unit impulse. What is its transfer function?

[3.0 Marks]

Table Q2-a)

Characteristic Table: UV Flip-Flop		
U	V	Q(t+1)
0	0	0
0	1	Q'(t)
1	0	Q(t)
1	1	1

Table Q2-b)

Present state	Next state		Output	
	x = 0	x = 1	x = 0	x = 1
a	b	a	0	0
b	c	a	0	0
c	d	a	0	0
d	d	a	1	1

	X_1X_2 00	01	11	10
a	ⓐ, 1	ⓐ, 1	b , -	c , -
b	c , -	ⓑ, 1	ⓑ, 1	ⓑ, 1
c	ⓒ, 0	d , -	ⓒ, 0	ⓒ, 0
d	a , -	ⓓ, 0	c , -	ⓓ, 0

Figure Q3-a)

	X_1X_2 00	01	11	10
a	c	ⓐ	b	b
b	ⓑ	c	ⓑ	ⓑ
c	ⓒ	ⓒ	b	b

Figure Q3-c)

Table Q4-b)

Parameter	Name	NAND gate	NOR gate
V_{CC}	Supply voltage	5V	5V
I_{CCH}	High-level supply current of a single gate	2.5mA	3.2mA
I_{CCL}	Low-level supply current of a single gate	5.0mA	5.4mA
V_{OH}	High-level output voltage	2.7V	2.7V
V_{OL}	Low-level output voltage	0.5V	0.5V
V_{IH}	High-level input voltage	2V	2V
V_{IL}	Low-level input voltage	0.8V	0.8V
I_{OH}	High-level output current	1mA	0.4mA
I_{OL}	Low-level output current	20mA	8mA
I_{IH}	High-level input current	0.05mA	20μA
I_{IL}	Low-level input current	2mA	0.4mA
t_{pLH}	Low-to-high delay	3ns	13ns
t_{pHL}	High-to-low delay	3ns	10ns

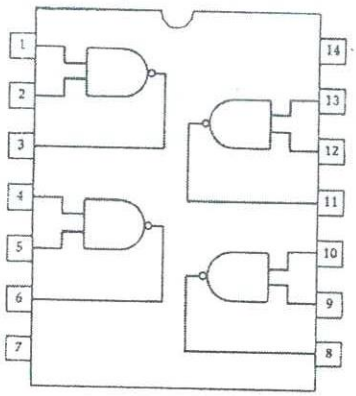

Figure Q4-b)

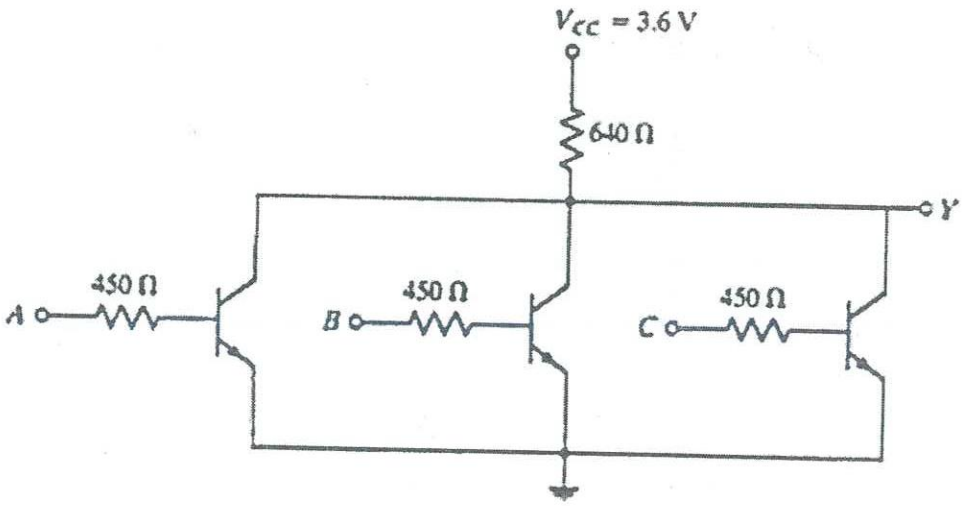

Figure Q4-c)