UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5, Examination in Engineering, Aug 2014

Module No: EE5316 **Module Name: Computer Architecture and Operating Systems**

[Two Hours]

[Answer all questions. Each question carries 10 marks]

Part II

Q1. a) State main concepts of John von Neumann Architecture. [2 Marks]

b) Draw the block diagram of a typical top level architecture of Jon von Neumann computer. Show all major constituents. [2 Marks]

c) What is memory and logic performance gap in modern computers? [1 Marks]

d) Name 3 architectural solutions aimed to minimize the effect of the memory and logic performance gap. [1 Marks]

e) Consider a linearly organized byte-wise addressable 64 Kbytes of memory device.

i. What is the required width of address bus?

ii. What is the minimum width of data bus?

iii. If the control bus is made of R/W signal which is high for read operations and low for write operations, describe the step by step CPU actions on the system bus when executing a write operation. You may also use appropriate timing diagrams.

[3 Marks]

f) Draw the internal architecture of a typical 16 MByte DRAM organized in 8-bit cell arrays in a block diagram. Show the identified size of a cell array, widths of address and data buses, and necessary control bus signals. [1 Marks]

Q2. a) State the principle of locality of reference. [2 Marks]

b) Show the structure of Cache and Main memory in a block diagram indicating the Direct Mapping parameters; Word, Block, Line and Tag. [2 Marks]

c) Consider the hypothetical 8 byte memory which is connected to the CPU through 4 Bytes of Cache memory, having 2 Lines of size 2 Words. Size of Word is 1 Byte.

i. How to identify the Word, Block, and Tag by using the memory address? .

ii. What is the Tag, Line and Word for the Memory address 5?

[2 Marks]

d) A program consists of 10000 Bytes and resides in Main Memory, which is connected through cache. The CPU found 9500 of program bytes in Cache during the first hit, while other 500 had to be loaded from Main memory after checking in Cache. Cache Memory and Main Memory access times are $0.01[\mu s]$ and $0.1[\mu s]$, respectively.

i. Draw a graph to indicate the successful cache hit rate H [%] vs average memory access time T_{avr} $[\mu]$.

ii. What is the average time needed to load a byte during the execution of the complete program?

[4 Marks]

Q3. Instruction pipeline of a certain processor has 6 stages.

FI - Fetch Instruction
DI - Decode Instruction
CO - Calculate Operands
FO - Fetch Operands
EI - Execute Instructions
WR - Write Results

a) Draw the timing diagram for the instruction pipeline operation for 9 instructions, assuming no branches. [2 Marks]

b) Derive the general formula for the total time required to execute n instructions by the pipeline as a function of pipeline cycle time T and number of pipeline stages k. [2 Marks]

c) Derive the formula for pipeline speedup S defined as

$$S = \frac{\text{Total Time Required to Execute } n \text{ Instructions without Pipeline}}{\text{Total Time Required to Execute } n \text{ Instructions with Pipeline}}$$

[2 Marks]

d) Calculate the speedup for 25000 instructions. [2 Marks]

e) What will happen if 3-rd instruction is a branch instruction. Describe by using a timing diagram. [2 Marks]