UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 3 Examination in Engineering: February 2023

Module Number: EE3301 **Module Name: Analog Electronics (C-18)**

[Three Hours]

[Answer **all questions**, each question carries 10 marks]

[Attach the question paper to your answer script. Failing which, you will get zero for Q3]

Q1 a) State three FET biasing mechanisms.

[2 Marks]

b) Draw the voltage divider biasing circuit for a N- Channel JFET.

[2 Marks]

c) Figure Q1 shows a biased stabilized JFET amplifier with $g_m = 2mS$, $r_{ds} = 30\ k\Omega$, $R_S = 3k\Omega$, $R_D = R_L = 2k\Omega$, $R_1 = 200k\Omega$, $R_2 = 800k\Omega$ and $r_i = 5k\Omega$. The values of C_C and C_S are large and the amplifier is biased in the pinch off region.

i) Draw the small signal equivalent circuit.

ii) Find Z_{in}

iii) Find $A_v = v_L/v_i$

iv) Find $A_i = i_L/i_i$

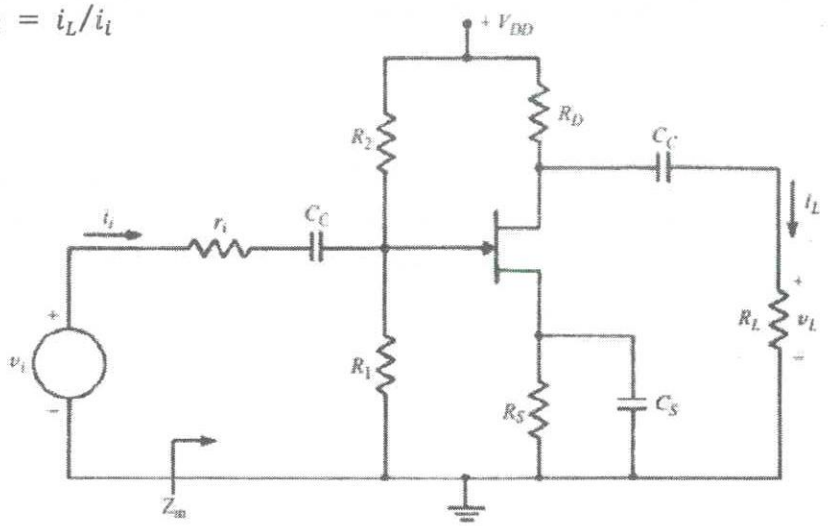

Figure Q1

[5 Marks]

d) What is the purpose of C_S capacitor in Figure Q1 circuit diagram?

[1 Mark]

Q2 a) Briefly explain the importance of current mirrors in analog IC designs.

[1 Mark]

b) Figure Q2 shows a basic current mirror. Prove that the source current I in the circuit is mirrored to the collector current of transistor T2.

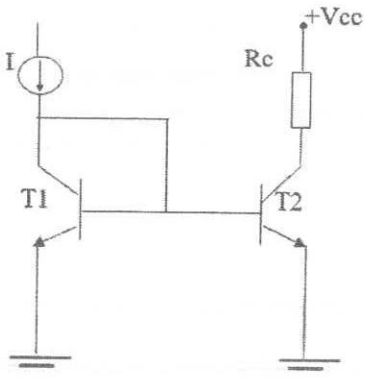

Figure Q2

[2 Marks]

c) i) Draw the circuit diagram of an ideal differential amplifier that has a collector resistors R_C , bias voltage $+V_{CC}$ and a constant current source I.

ii) Perform DC analysis for the circuit to derive expressions for the DC output voltages.

[3 Marks]

d) A BJT differential amplifier is biased from a 1 mA constant current source and includes a 200 Ω resistor in each emitter. The collectors are connected to V_{CC} via 12 kΩ resistors. A differential input signal of 0.1 V is applied between the two bases. Find the currents in the emitter i_e and the voltage v_{be} for each BJT

[4 Marks]

Q3 Answer Q3 in the space provided and attach the question paper to your answer script.

a) Complete the circuit shown in Figure Q3a in the space provided, to receive the output $v_{out} = -(v_1 + v_2 + v_3)$ where v_1, v_2, v_3 are inputs. The feedback resistor value, R_f = 10 kΩ. Clearly mark the resistors and voltages in the diagram.

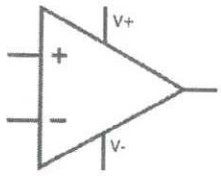

Figure Q3a

[2 Marks]

b) For the following questions **circle ONE answer** that best fits the questions.

[8 Marks]

i) Find the output V_o shown in the circuit in Figure Q3b – i. Assume an ideal op-amp.

A) – 3.8 V B) – 5.7 V C) – 0.3428 V D) 0.3428 V E) None of the above

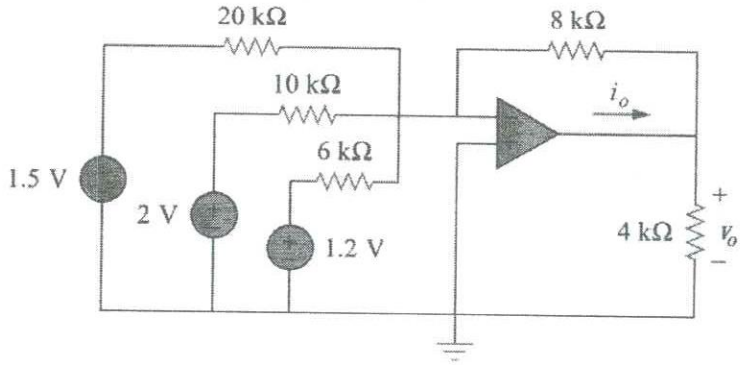

Figure Q3b – i

ii) Find the output voltage V_o in the circuit shown in Figure Q3b – ii.

A) – 1 V B) 6 V C) – 7 V D) – 6 V E) Insufficient Information

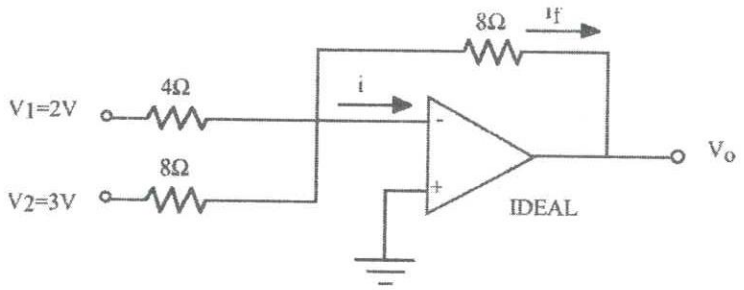

Figure Q3b – ii

iii) For the difference amplifier circuit shown in Figure Q3b – iii, determine the output voltage at terminal A.

A) 6.07 V B) – 15.45 V C) – 18.13 V D) – 6.07 V E) – 3.54 V

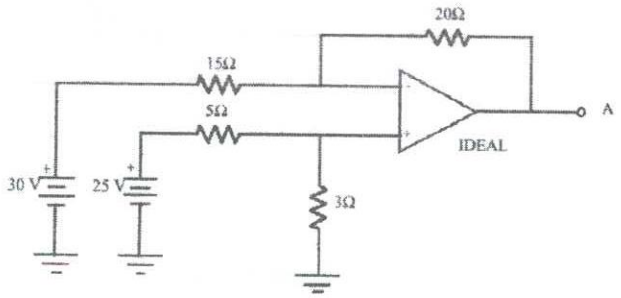

Figure Q3b – iii

iv) The output of an op-amp increases 8 V in 12 μs. The slew rate is _____.

A) 1.5V/μs B) 0.6 V/μs C) 96 V/μs D) 0.667 V/μs E) None of these

v) For an op-amp with negative feedback, the output is _____.

A) Magnitude is decreased
B) Fed back to the inverting input
C) Equal to the input
D) Increased
E) Fed back to the non-inverting input

vi) Op-amp integrator uses _____ as a feedback element.

A) Inductor
B) A simple wire
C) Capacitor
D) Resistor
E) Any of the above

vii) Find the input voltage of an ideal op-amp if one of the inputs is 2 V and the output is 12V, with a gain of 3.

A) - 4 V
B) - 2 V
C) 8 V
D) 4 V
E) None of the above

viii) The common-mode gain of op-amp should be _____.

A) Always unity
B) Unpredictable
C) Very high
D) Very low
E) Not enough information

ix) In differential-mode, _____.

A) The outputs are of different amplitudes
B) The outputs are of different polarities
C) Opposite polarity signals are applied to the inputs
D) The gain is unity
E) Only one supply voltage is used

x) An op-amp can amplify _____.

A) DC signals only
B) AC signals only
C) Neither AC nor DC signals
D) Both AC and DC signals
E) Not sufficient information

xi) A voltage follower _____.

A) Has no feedback resistor
B) Has a voltage gain of 1
C) Is non-inverting
D) Has all of the above A, B and C
E) Has none of the above A, B or C

xii) The ideal op-amp has the following characteristics

A) $R_{in} \rightarrow \infty$, $Av \rightarrow \infty$, $R_{out} = \infty$
B) $R_{in} \rightarrow 0$, $Av \rightarrow \infty$, $R_{out} = \infty$
C) $R_{in} \rightarrow \infty$, $Av \rightarrow \infty$, $R_{out} = 0$
D) $R_{in} \rightarrow 0$, $Av \rightarrow \infty$, $R_{out} = 0$
E) None of the above

xiii) A common mode signal is applied to _____.

A) Both inputs
B) One of the inputs
C) The non-inverting input
D) The inverting input
E) Top of the tail resistor

xiv) A non-inverting amplifier has R_{in} = 1 kΩ and R_f=100 kΩ. The closed-loop voltage gain is _____.

A) 100 B) 1.01 C) 1000 D) 101 E) 0.01

xv) When a step-input is given to an op-amp integrator, the output will be a _____.

A) Rectangular Wave
B) Triangular Wave
C) Ramp
D) Sinusoidal Wave
E) Not enough information

xvi) For an op-amp having differential gain A_v and common mode gain A, the Common Mode Rejection Ratio (CMRR) is given by _____.

A) A_v+1/A
B) A/A_v
C) A_v+A
D) A_v/A
E) None of the above

Q4 a) Predict how the operation of this operational amplifier circuit shown in Figure Q4a will be affected as a result of the following faults. Consider each fault independently (i.e. one at a time, no multiple faults occurring simultaneously).

i) Resistor R2 fails open:
ii) Solder bridge (short) across resistor R2:
iii) Resistor R1 fails open:
iv) Solder bridge (short) across resistor R1:
v) Broken wire between R1/R2 junction and inverting opamp input:

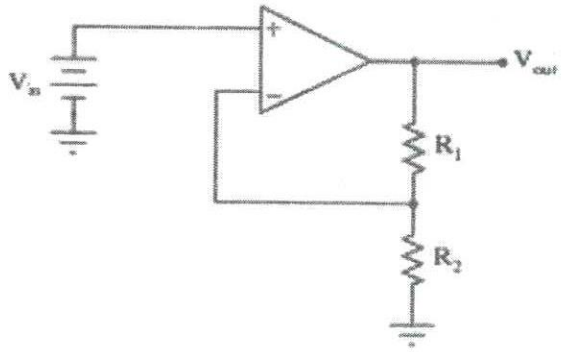

Figure Q4a

[5 Marks]

b) Figure Q4b shows an op-amp circuit.

i) Calculate the output voltage V_{out}.
ii) Calculate the voltage drops across resistors R_1 and R_2.
iii) Calculate the overall voltage gain of this amplifier circuit (given by A), both as a ratio and in units of decibels (dB):

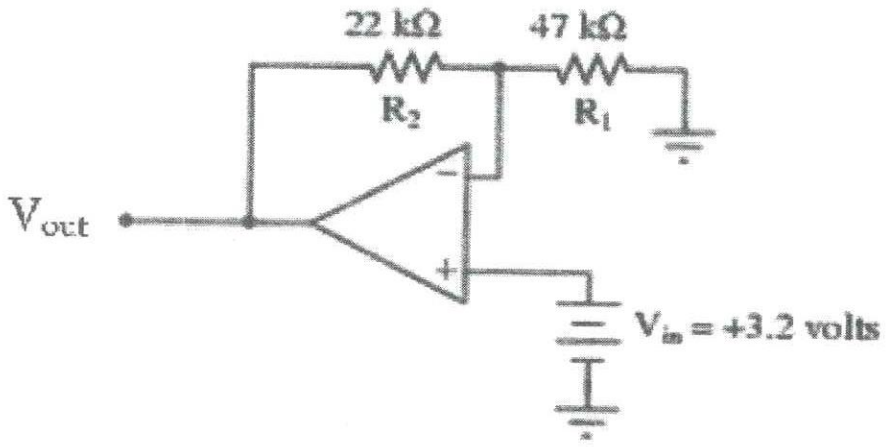

Figure Q4b

[5 Marks]

Q5 a) Answer each of the following in relation to analog filters.

i) Explain the difference between high pass filter and a notch filter.

ii) Explain the difference between passive analog filters and active analog filters, mentioning the components that are used.

iii) What does a bode plot indicate?

[5 Marks]

b) Find the bandwidth of the given filter in Figure Q5 and draw the amplitude response marking the cut off frequencies. C = 1.5 nF, R_1=10 kΩ, R_2 = 1 kΩ.

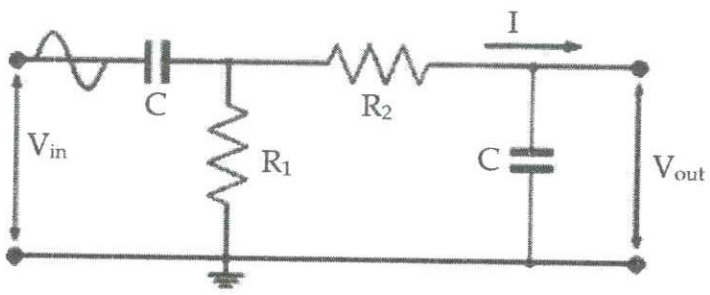

Figure Q5

[5 Marks]