UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5 Examination in Engineering: May 2023

Module Number: EE5201 **Module Name: Computer Architecture**

[Three Hours]

[Answer **all questions**, each question carries 12.5 marks]

Q1 a) Briefly describe the following.

i) Instruction set architecture.

ii) Micro architecture.

[1 Mark]

b) Briefly explain (in point form) how the introduction of integrated circuits (Large Scale Integration) has immensely assisted the development of computers.

[1 Mark]

c) The architecture of an IAS computer is given in Figure Q1a, of which the instruction cycle consists of four stages, namely; fetch instruction, decode instruction, fetch operand and execute instruction. Briefly explain in point form the operation of each of the stages along with the associated registers.

[4 Marks]

d) A subset of instructions used in the IAS computer is given in Figure Q1b and the format of a word is given in Figure Q1c. Note that the lefthand side instruction is executed first.

i) List the symbolic representation of the instructions associated with the two words given below.

00001001100010001010000010100000000000000
00000110000010001000001000010000010001010

[2.5 Marks]

ii) Referring to the memory occupancy given in Figure Q1d, list the values of important registers and memory addresses after the execution of each instruction identified in part i).

[4 Marks]

Q2 a) Pipelining and GPUs are introduced to improve the performance of modern computers. Briefly explain in point form the difference between the two approaches.

[2 Marks]

b) Suppose that a processor with 2 Kbytes of cache is plugged into a computer with 4 Gbytes of main memory. The cache memory consists of 8-byte offset and it employs 4-way set associative cache mapping.

i) Briefly describe two main cache write policies.

[2 Mark]

ii) Calculate the number of sets associated with the cache memory. Clearly show each step of your calculations.

[2 Marks]

iii) Suppose that only the third hexadecimal digit of the below memory address is clearly visible. Identify the range of sets that the memory address can be mapped to.

Memory Address: 0xYYYYYDYY (Y denotes an unknown hexadecimal digit)

Hint: Identify the bits representing the set ID and figure out the range of possibilities.

[2.5 Marks]

c) Suppose that you are to detect and correct single-bit errors in 6-bit data packets. A data packet which is encoded with a Hamming code is retrieved as 0011001101. Find the original 6-bit data packet using appropriate equations among the ones given below. Clearly show each step of your calculation.

$$P_1 = D_3 \oplus D_5 \oplus D_7 \qquad P_1 = D_3 \oplus D_5 \oplus D_7 \oplus D_9 \oplus D_{11}$$

$$P_2 = D_3 \oplus D_6 \oplus D_7 \qquad P_2 = D_3 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{11}$$

$$P_4 = D_5 \oplus D_6 \oplus D_7 \qquad P_4 = D_5 \oplus D_6 \oplus D_7 \oplus D_{12}$$

$$P_8 = D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12}$$

[3 Marks]

d) State two advantages and two disadvantages of solid-state drives (SSD) over spinning disks.

[1 Marks]

Q3 a) What is the main problem of shared busses that is addressed by Point-to-Point interconnect technology.

[2 Marks]

b) The 1x PCIe 3.0 card supports 1 Gbps data rate and subsequently 4x and 16x PCIe 3.0 cards support data rates of 4 Gbps and 16 Gbps, respectively. Suppose that a motherboard consists of four 4x PCIe 3.0 slots and you are given two 16x PCIe 3.0 cards. Giving reasons, calculate the cumulative data rate that can be achieved by the given setup.

[2 Marks]

c) A block diagram of an instruction cycle is given in Figure Q3. Suppose that the fetch stage takes 20 ns and the execute stage takes 25 ns and the instructions are executed in a pipeline.

i) If the interrupts are introduced to the system, re-draw the block diagram incorporating the interrupts.

[1 Mark]

ii) Suppose that there are 20 instructions in a program. Calculate the speedup of the processor.

[2 Marks]

iii) Suppose that there is a comment from one of your colleagues that more realistic speedup would be close to 1.71 when the time durations are considered. Discuss in point form the validity of this statement, by giving appropriate reasoning/calculations.

[2 Marks]

iv) Suppose that an instruction is a branch instruction with a probability q and branch prediction is successful with a probability of p. Derive an equation for speedup of the pipeline in running N instructions.

Hint: Ignore the durations of pipeline stages

[2 Marks]

v) Identify the pipeline hazard associated with this pipeline by giving reasons.

[1.5 Marks]

Q4 a) Two's (2's) complement representation is commonly used to work with negative numbers

i) Carry out the binary subtraction 10110 – 11011 using 8-bit registers and 2's complements representation. Show each step of your calculation giving reasons.

[1.5 Mark]

ii) The 2's complement representation of two numbers are given below as X and Y. Carryout the binary addition of two numbers.

X = 1111 1111 1101 1011 Y = 1111 0011

[2 Marks]

b) Carry out the binary multiplication 8 x 9 using the algorithm given in Figure Q4a and template given in Figure Q4b. Clearly show each step of your calculation.

[2 Marks]

c) Briefly explain in point form the disadvantages of uniform memory access overcame by introducing non-uniform memory access (NUMA).

[2 Marks]

d) Consider a symmetric multiprocessor system given in Figure Q4c.

i) Calculate the speedup of the system when executing 1000 instructions out of which 600 can be executed in parallel.

[1 Mark]

ii) If this symmetric multi-processor system is used instead of a single processor which is twice as fast as the processors in multiprocessor system, calculate the speedup of the multiprocessor system.

$$\text{Speedup} = \frac{\text{Time to execute the program on a single processor}}{\text{Time to execute the program on parallel processors}}$$

[2 Marks]

iii) Identify the minimum number of processors required in the symmetric multi-processor system to outperform the single processor given in part ii), when executing the above set of instructions.

Hint: Derive an equation for the speedup and obtain an inequality using the fact that the speedup should be greater than 1.

[2 Marks]

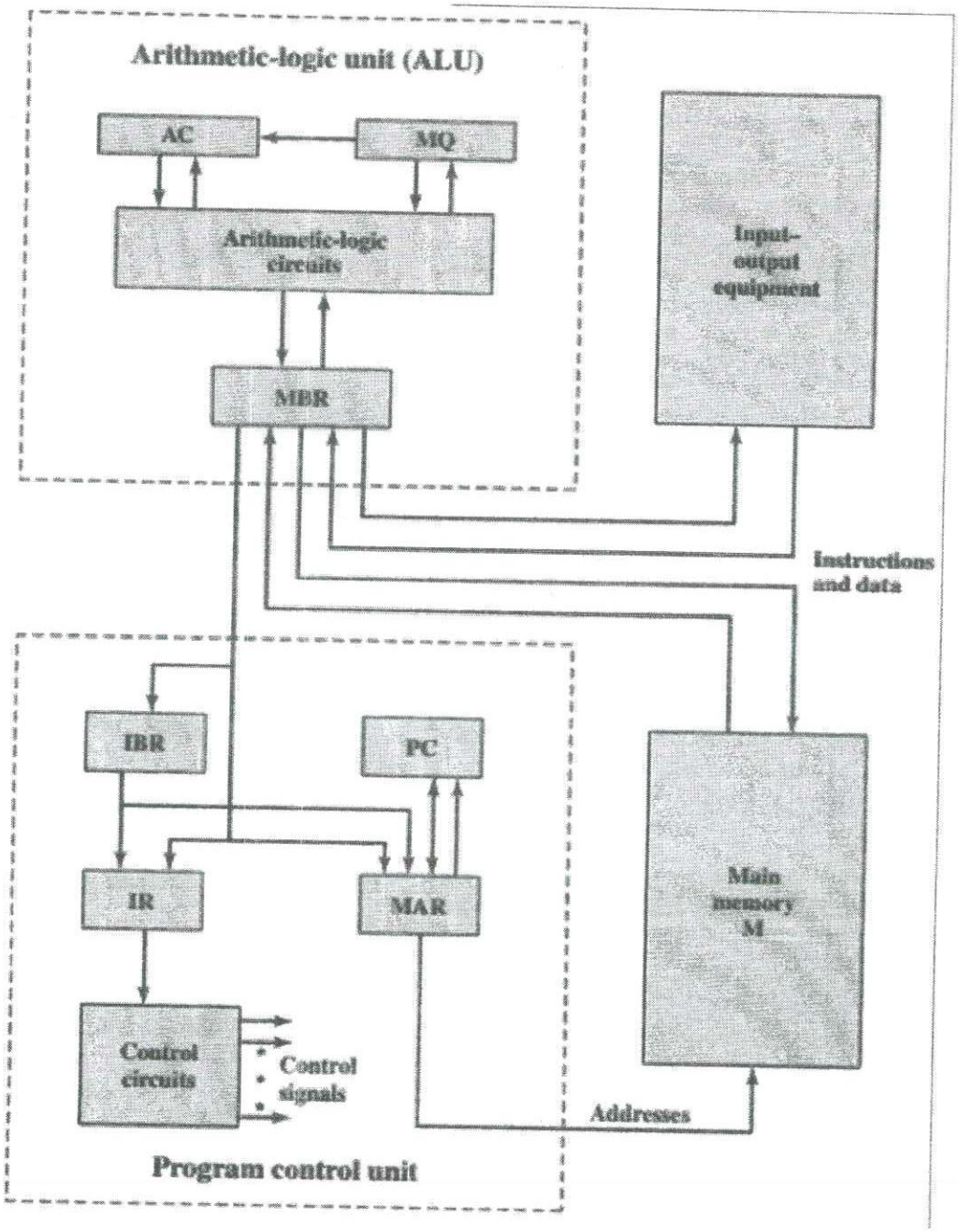

Figure Q1a: The architecture of an IAS computer

Instruction Type	Opcode	Symbolic Representation	Description
Data transfer	00001010	LOAD MQ	Transfer contents of register MQ to the accumulator AC
	00001001	LOAD MQ,M(X)	Transfer contents of memory location X to MQ
	00100001	STOR M(X)	Transfer contents of accumulator to memory location X
	00000001	LOAD M(X)	Transfer M(X) to the accumulator
	00000010	LOAD -M(X)	Transfer -M(X) to the accumulator
	00000011	LOAD |M(X)|	Transfer absolute value of M(X) to the accumulator
	00000100	LOAD -|M(X)|	Transfer -|M(X)| to the accumulator
Unconditional branch	00001101	JUMP M(X,0:19)	Take next instruction from left half of M(X)
	00001110	JUMP M(X,20:39)	Take next instruction from right half of M(X)
Conditional branch	00001111	JUMP + M(X,0:19)	If number in the accumulator is nonnegative, take next instruction from left half of M(X)
	00010000	JUMP + M(X,20:39)	If number in the accumulator is nonnegative, take next instruction from right half of M(X)
Arithmetic	00000101	ADD M(X)	Add M(X) to AC; put the result in AC
	00000111	ADD |M(X)|	Add |M(X)| to AC; put the result in AC
	00000110	SUB M(X)	Subtract M(X) from AC; put the result in AC
	00001000	SUB |M(X)|	Subtract |M(X)| from AC; put the remainder in AC
	00001011	MUL M(X)	Multiply M(X) by MQ; put most significant bits of result in AC, put least significant bits in MQ
	00001100	DIV M(X)	Divide AC by M(X), put the quotient in MQ and the remainder in AC
	00010100	LSH	Multiply accumulator by 2; that is, shift left one bit position
	00010101	RSH	Divide accumulator by 2; that is, shift right one position

Figure Q1b: Instruction set used in IAS computer

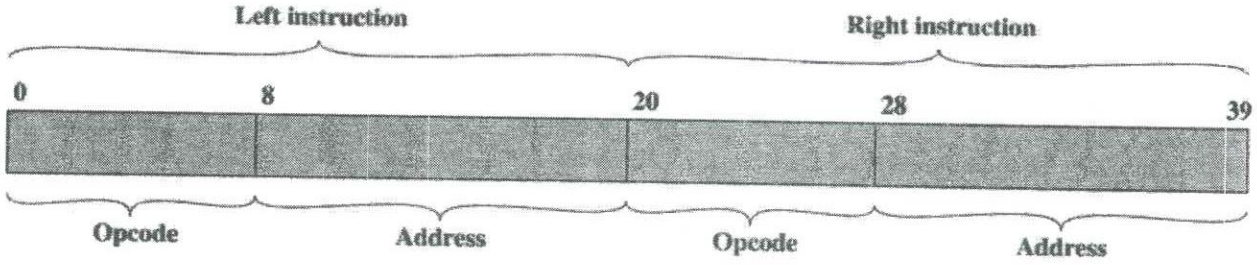

Figure Q1c: Word Format of an IAS computer

Address	Data
2185	60
2186	50
2187	40
2188	30

Address	Data
0135	10
0136	20
0137	30
0138	40

Figure Q1d: Memory occupancy

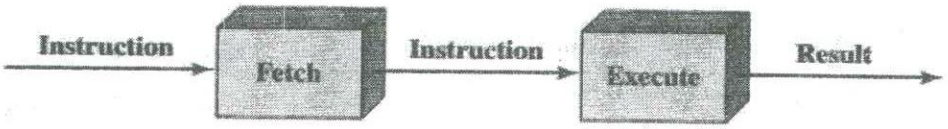

Figure Q3

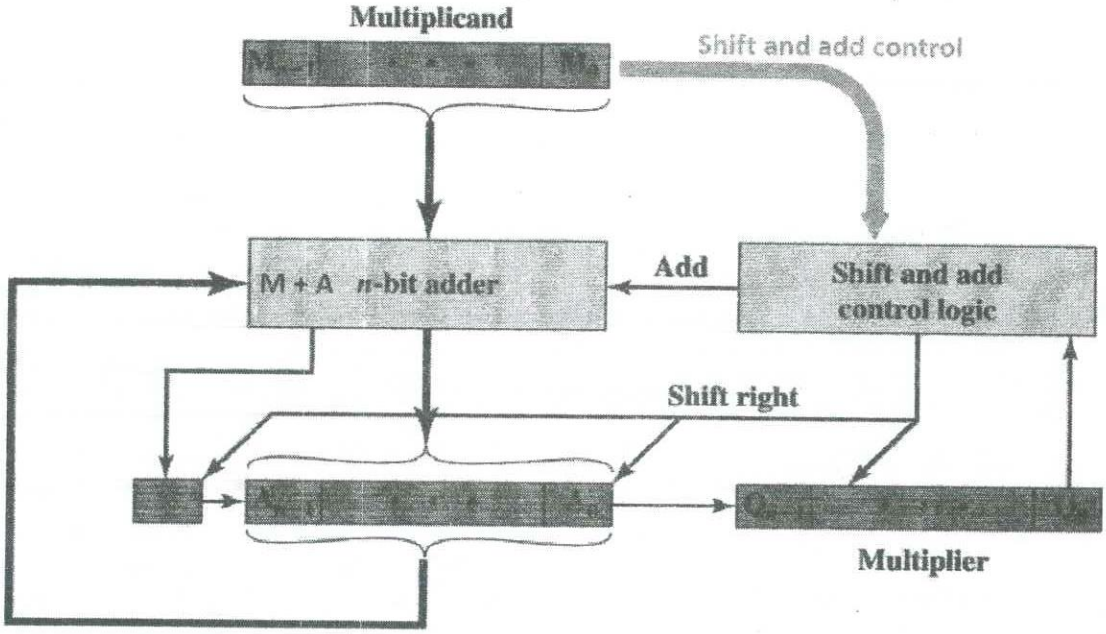

Figure Q4a: Block diagram of the multiplication algorithm

C		A					Q					M			
							1	0	0	0		1	0	0	1

Figure Q4b: Template of the calculation

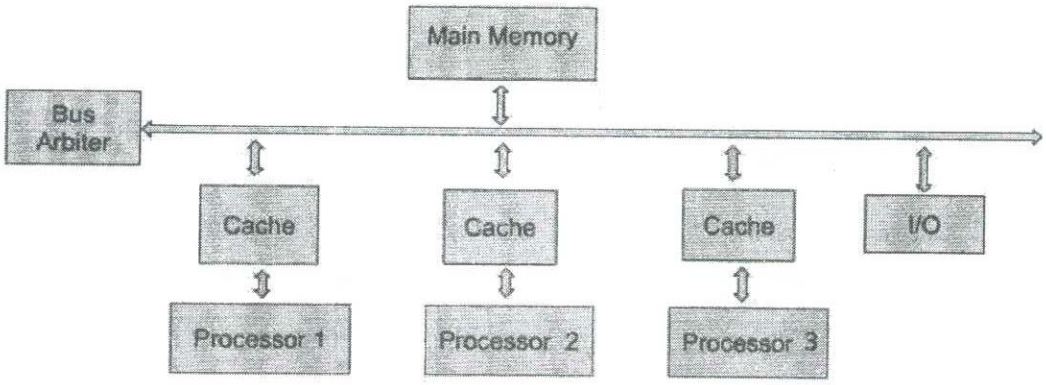

Figure Q4c: Symmetric multiprocessor system