University of Ruhuna- Faculty of Technology

Bachelor of Engineering Technology Honours Degree
Level 4 (Semester II) Examination, December 2023
Academic year 2021/2022

Course Unit: ENT 4212 – Programmable Digital Electronics Design

Duration: 2 hours

- All symbols have their usual meanings.
- This paper contains **five (05)** questions on **five (05)** pages.
- Answer **all** the questions.
- This is a **closed book** examination.

Q1.

i. Briefly explain the terms "combinational logic" and "sequential logic" in digital electronic design. (4 marks)

ii. Draw the logic circuit diagrams for implementing the following digital functions.

a). A three input NAND gate using two input NAND gates. (3 marks)

b). A NOT circuit using a two input NOR gates. (2 marks)

iii. What is a Simple Programmable Logic Device (S-PLD)? (2 marks)

iv. State the main differences between Programmable Array Logic (PAL), Programmable Logic Array (PLA), and Programmable Read Only Memory (PROM) According to their programmability. (3 marks)

v. $F(w,x,y) = \sum (2, 6, 4, 3)$

a). Write down a Boolean function for F. (3 marks)

b). Draw the Karnaugh map for F and simplify the Boolean function for F. (3 marks)

Q2.

i. Briefly explain the meaning of rise time / fall time in digital logic. (2 marks)

ii. List down 4 characteristics of an ideal logic family. (2 marks)

iii. A combinational logic circuit is shown in the following Figure 1. Assume the propagation time delay of each gate is linearly proportional to the number of inputs in the gate.

(Example: delay of a gate with two inputs is 2ns).

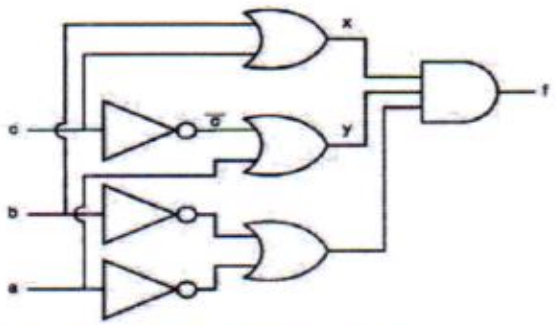

Figure 1 Combinational logic circuit for Q2

a). Compute the longest propagation time delay. (2 marks)

b). Compute the maximum possible frequency of operation of this circuit. (2 marks)

iv. The table below, shows the data sheet of an IC comprising logic gates.

Parameter	Name	Value
Vcc	Supply voltage	5V
I_{CCH}	High level supply current	10mA
I_{CCL}	Low level supply current	20mA
V_{OH}	High level output voltage (min)	2.7V
V_{OL}	Low level output voltage (max)	0.5V
V_{IH}	High level input voltage (min)	2V
V_{IL}	Low level input voltage (max)	0.8V
I_{OH}	High level output current (max)	1mA
I_{OL}	Low level output current (max)	20mA
I_{IH}	High level input current (max)	0.05mA
I_{IL}	Low level input current (max)	1mA
t_{PLH}	Low-to-high delay	3ns
t_{PHL}	High-to-low delay	3ns

Calculate the following quantities of the above IC.

a). Fan-out
b). Power dissipation
c). Propagation time Delay
d). Noise Margin

(4*3=12 marks)

Q3.

You are supposed to design a digital system for a Biomedical instrument fulfilling the following requirements.

- Temperature, blood pressure, pulse rate and respiration rate should be measured using separate sensors.
- If at least one of the above 4 measurements exceeds a predefined value, an alarm should ring.
- If both blood pressure and respiration rate exceed the predefined values, the ventilation system should start automatically.

i. Identify the inputs and outputs of the system. (4 marks)

ii. What is the PLD type that you should use in this design project? (2 marks)

iii. Explain 2 advantages of using the selected PLD type. (4 marks)

iv. Draw the truth table and the PROM circuit diagram for the above case. (10 marks)

Q4.

i. Draw a circuit diagram for Diode Logic AND gate and explain the working principle of it. (4 marks)

a) List 4 issues associated with the Diode Logic Circuits. (4 marks)

b) Explain why TTL gate is much faster than DTL. (3 marks)

ii. Differentiate FPGA and ASIC. (3 marks)

iii. Determine the programmable interconnections in the following programmable logic devices.

a). 2K x 4 PROM (3 marks)

b). PLA device with eight input variables, 16 AND gates, and 4 OR gates. (3 marks)

Q5.

A line following robot must be designed with the following specifications.

- If the two center sensors (S2 and S3) detect the line while the outer sensors (S1 and S4) do not, the robot continues moving straight ahead.
- If one of the center sensors detects the line (S2 or S3) while the other doesn't, according to the outer sensor inputs, the robot may turn in the direction of the sensor detecting the line to realign itself with the path.
- If both center sensors detect the line and any outer sensor detects the line at the same time, both motors switch off.
- If both outer sensors detect the line simultaneously, both motors need to switch off.
- If only one center sensor detects a line with no other detections in outer sensors, both motors need to stop.

- The robot has two independent Motors (connected to wheels) to generate motion.
  - Both motors (M1 & M2) on – Forward motion
  - Left motor(M1) on, right motor(M2) off – Right turn
  - Left motor off(M1), right motor(M2) on – Left turn
  - Both motors (M1 & M2) off – No motion

- Figure 2 shows the sensors and motors alignment.

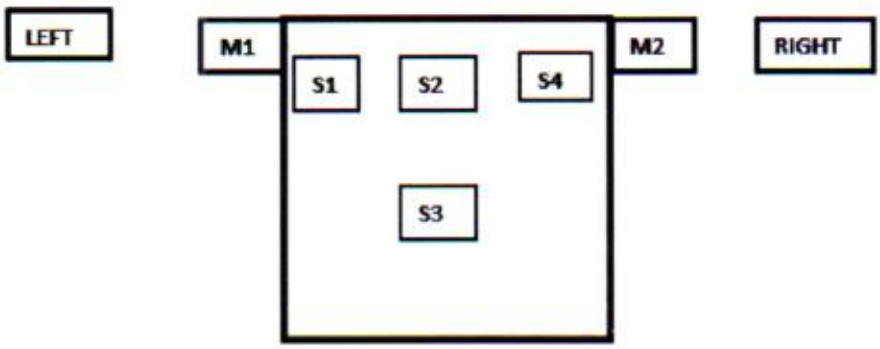

Figure 2 Sensors and motors alignment for Q5.

A digital combinational control circuit takes the sensor outputs logical values as inputs and outputs logic signals to the motors.

i. Define the different inputs and outputs with suitable logic values. (4 marks)

ii. Draw a truth table for the above inputs and outputs. (4 marks)

iii. Generate the Boolean expressions for the above truth table (SOP) and simplify them. (4 marks)

iv. Draw a timing diagram for the above truth table. (4 marks)

v. Write down a Verilog source code for the simplified Boolean expressions of M1 and M2. (4 marks)

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