University of Ruhuna- Faculty of Technology

Bachelor of Engineering Technology Honours Degree
Level 2 (Semester II) Examination, December 2023
Academic year 2021/2022

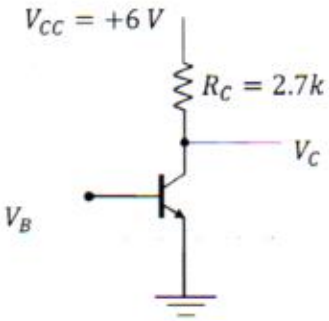
Course Unit: ENT2213 Digital Electronic Systems

Time Allowed: 3 hrs

- All symbols have their usual meanings.
- Answer **all six(06)** questions.
- Use Annexure 1 and 2 to answer the relevant questions.

1.

a. The following circuit can operate as a two-level system that can generate HIGH and LOW states of output over a continuous input voltage. Briefly discuss the working principle of the following circuit generating HIGH and LOW logic states. [2 marks]



b. Write the decimal number 627 in following forms.
   i. Binary representation. [2 marks]
   ii. Octal representation. [2 marks]
   iii. Hexadecimal representation. [2 marks]

c. Digital electronic is based on operating logical functions in binary representation of input signals and alphanumeric characters.
   i. What would you understand by the acronyms LSB and MSB in a 8-bits binary number. [1 mark]
   ii. Briefly, discuss the need and the importance of Octal and Hexadecimal representations in digital electronics. [1 mark]

2.

a. Define the terms "Combinational Logic" and the "Sequential Logic" in digital electronics. [2 marks]

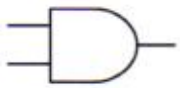
b. Define the operation of the gates NOR, and NAND by writing the,
   i. Truth Table. [1 mark]
   ii. Boolean expression. [1 mark]

c. Sketch the logic circuit diagram for the following Boolean expression. [2 marks]

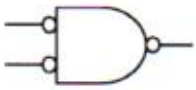
$$Y = A.B + A.\bar{B}.\bar{C} + A.\bar{C}$$

d. In digital electronic, the Active-High logic consider the High voltage state as logical True(T) state, whereas the Active-Low logic consider the High voltage state as logical False(F) state and vice- versa.
Construct the truth table for following gates and express the function of logic gates in Active-High and Active-Low logic.
(Note: Use the letter **T** for the **True** state and **F** for the **False** state.)

i. [2 marks]



ii. [2 marks]



3.

a. Use Boolean Algebra to show that [4 marks]

$$A + B.C = (A + B).(A + C)$$

b. Using the distributive law in part (a.) above, express the following equation in product of sum form with 4 product terms, each with a sum of 3 variables. [6 marks]

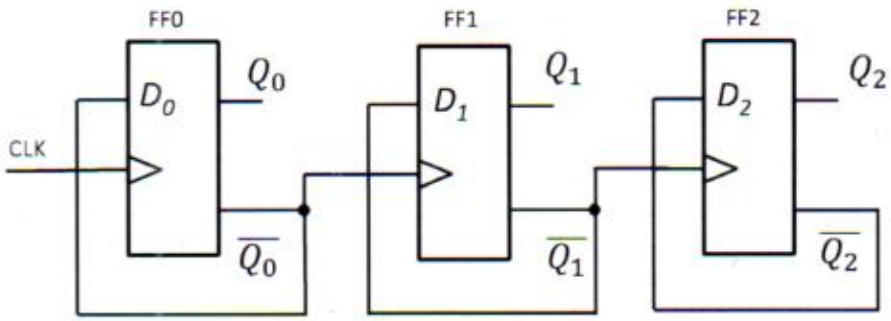
$$F = H + I.\bar{J} + \bar{K}.L$$

4. Implement the following Boolean function,

$$X = \bar{A}.\bar{B}.\bar{C} + B.\bar{C} + B.C$$

i. using a 8:1 Multiplexer. [4 marks]
ii. using a 4:1 Multiplexer plus a NOT gate. [4 marks]
iii. using a 2:1 Multiplexer plus a NOT gate and an OR gate. [2 marks]

5. The following figure shows a 3-bit Asynchronous counter.



a. Construct the timing diagram for the binary output of Q_0, Q_1 and Q_2 and explain the working of the counter. Assume all the flip-flops are reset to 0 initially. [3 marks]
(Use the provided space in Annexure 1 to draw the timing diagram)

b. For an industrial application, it is required to count from 1 to 6 repeatedly. Drawing the circuit diagram, explain how you would modify the above 3-bit asynchronous counter for this purpose. (Note: Consider the D-flip-flops have active-High set and reset controllers.) [4 marks]

c. The flip-flops have a propagation time delay. The propagation time delays of D-flip-flops are $T_{PLH} = T_{PHL} \approx 12\ ns$ and the propagation time delays of basic logic gates are negligible.

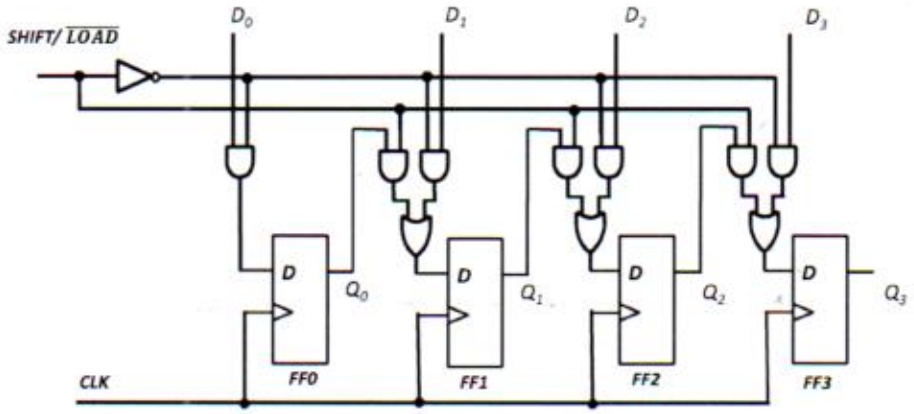
   i. What is the total propagation time delay of the above counter in part b. [2 marks]

   ii. Calculate the maximum clock frequency that the above counter can be operated. [1 mark]

6.

a. In digital Electronics what do you understand by the term "Shift Register"? [1 mark]

b. The following Figure shows a schematic circuit diagram of a Parallel In /Serial Out 4-bit shift register. Assume the flip flops are RESET initially.



i. Describe the operation of the above circuit when the logic sate of the SHIFT/LOAD input is LOW(0) and HIGH(1). [2 marks]

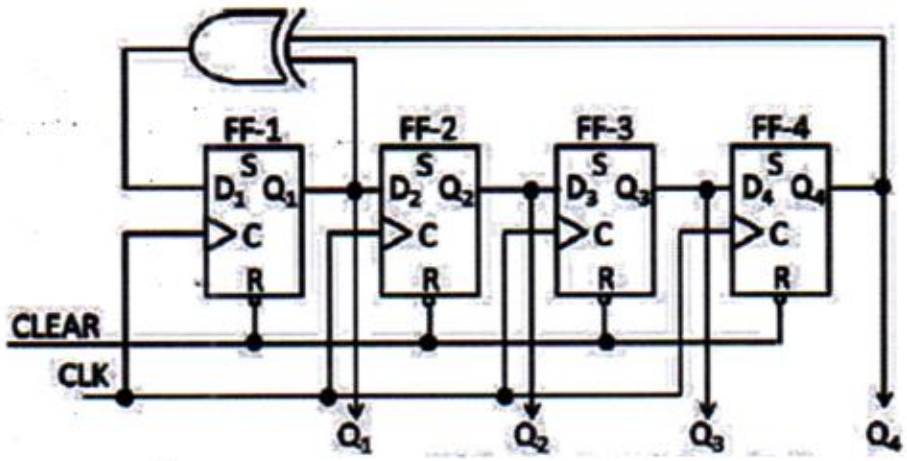
ii. Complete the following function table for the parallel data input of "1011" for D3, D2, D1 and D0 inputs respectively. [3 marks]

(Use the provided Table 6.b.ii. in Annexure 2)

Operation	CLOCK	input	Q_0	Q_1	Q_2	Q_3
CLEAR			0	0	0	0
SHIFT/LOAD=0	↑	D_0 =1 D_1 =1 D_2 =0 D_3 =1				
SHIFT/LOAD =1	↑					
	↑					
	↑					
	↑					

c. The following circuit shows the circuit diagram of a 4-bit Linear Feedback Shift Register (LFSR). S and R are Active-Low asynchronous set and reset controllers. Initially the flip-flop 1 (FF-1) is SET to HIGH(1) logic state and all the other flip-flops are RESET to LOW(0) logic state.

Describe the operation of the following LFSR by constructing the function table. [4 marks]



(Use the provided Table 6.c. in Annexure 2)

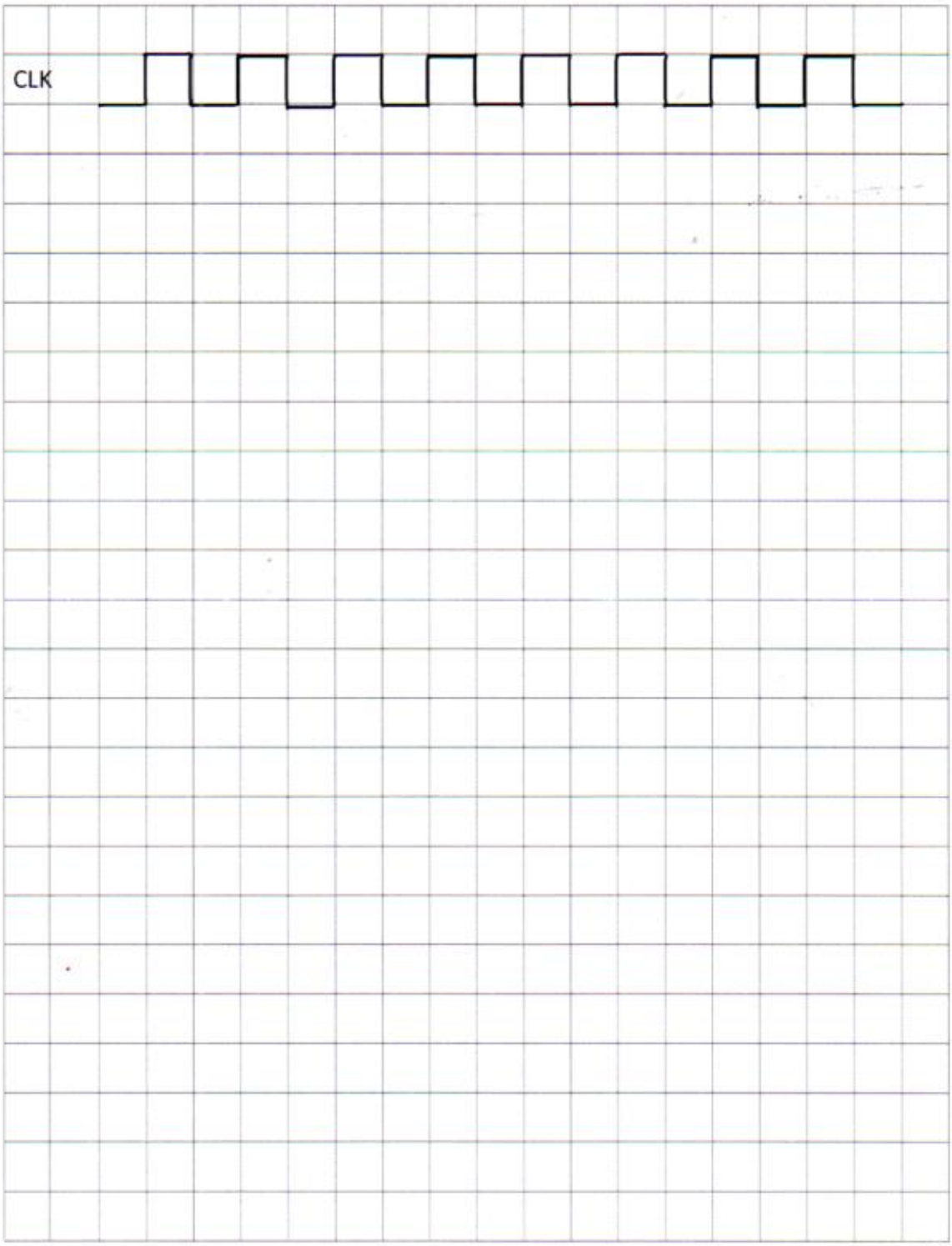
Operation	CLOCK	Q_1	Q_2	Q_3	Q_4
Initialize		1	0	0	0
CLOCK					

Laws and Rules in Boolean Algebra

1.	$X+0=X$	OR operations
2.	$X+1=1$	
3.	$X+X=X$	
4.	$X+\overline{X}=1$	
5.	$X.0=0$	AND operations
6.	$X.1=X$	
7.	$X.X=X$	
8.	$X.\overline{X}=0$	
9.	$\overline{\overline{X}}=X$	Double complement
10.	$X+Y=Y+X$	Commutative laws
11.	$XY=YX$	
12.	$(X+Y)+Z=X+(Y+Z)$	Associative laws
13.	$(X.Y).Z=X.(Y.Z)$	
14.	$X(Y+Z)=XY+XZ$	Distribution Law
15.	$X+Y.Z=(X+Y).(X+Z)$	Dual of Distributive Law
16.	$X+XZ=X$	Laws of absorption
17.	$X(X+Z)=X$	
18.	$X+\overline{X}Y=X+Y$	Identity Theorems
19.	$X(\overline{X}+Y)=X.Y$	
20.	$\overline{X+Y}=\overline{X}.\overline{Y}$	De Morgan's Theorems
21.	$\overline{X.Y}=\overline{X}+\overline{Y}$	

Annexure 1 Student's Registration No: .....

5. a. [3 marks]



Annexure 2 Student's Registration No: .....

6 b. ii. Function Table

Operation	CLOCK	input	Q_0	Q_1	Q_2	Q_3
CLEAR			0	0	0	0
SHIFT/LOAD=0	↑	D_0 =1 D_1 =1 D_2 =0 D_3 =1				
SHIFT/LOAD =1	↑					
	↑					
	↑					
	↑					

6 c. Function Table

Operation	CLOCK	Q_1	Q_2	Q_3	Q_4
Initialize		1	0	0	0
CLOCK					