UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 4 Examination in Engineering: September 2023

Module Number: EE4351 **Module Name: Digital Logic Design**

[Three Hours]

[Answer **all questions**, each question carries 10 marks]

Q1 a) State the difference between an encoder and a decoder in digital electronics.

[2 Marks]

b) Use Boolean algebra to simplify the following expression, then draw a logic gate circuit for the simplified expression:

$$\bar{A}\,\bar{B}\,\bar{C} + \bar{A}\,\bar{B}\,C + A\,\bar{B}\,\bar{C} + A\,\bar{B}\,C$$

Show all your working.

[2 Marks]

c) How many full adders are required to construct an m-bit parallel adder? Justify your answer.

[2 Marks]

d) A switching circuit has four inputs as shown in Figure Q1. A and B represent the first and second bits of a binary number N1. C and D represent the first and second bits of a binary number N2. The output will be 1, only if the product of the two numbers is less than or equal to 2 (N1 x N2 ≤ 2). Draw the truth table and find the minimized form of F using a Karnaugh Map.

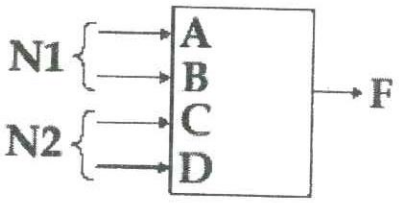

Figure Q1

[4 Marks]

Q2 a) State whether the following statements are TRUE or FALSE.

i) Two states are said to be equal if they have the same outputs.

ii) The switch which clears the flip-flop to its initial state is called clock.

iii) The state of the flip-flop can be switched by changing its input and output signals.

iv) Classification of sequential circuits depends upon their timing of signals.

[0.5x4 Marks]

b) Write the excitation table for JK flip flop.

[2 Marks]

c) A sequential circuit needs to be designed with two JK flip-flops, A and B, and two inputs, E and F, with the following specifications.

- If E = 0, the circuit remains in the same state regardless of the value of F.
- When E = 1 and F = 1, the circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats.
- When E = 1 and F = 0, the circuit goes through the state transitions from 00 to 11, to 10, to 01, back to 00, and repeats.

i) Obtain the state table.

[2 Marks]

ii) Determine the logic equation for each flip flop input.

[2 Marks]

iii) Draw the logic circuit.

[2 Marks]

Q3 a) State whether the following statements are TRUE or FALSE.

i) The SR latch consists of two cross coupled NAND gates or NOR gates.
ii) Memory elements in asynchronous circuits are clocked flip flops.
iii) Asynchronous sequential logic circuits usually perform operations in fundamental mode.
iv) Asynchronous sequential logic circuits are used when the primary need is speed.

[0.5x4 Marks]

b) Briefly explain the critical race condition in asynchronous logic circuits.

[2 Marks]

c) Consider the flow table given in Figure Q3.

	x_1x_2 = 00	01	11	10
a	(a)	b	c	(a)
b	a	(b)	(b)	c
c	a	(c)	(c)	(c)

Figure Q3

i) Obtain the transition diagram for this flow table.
ii) Show that it is not possible to make a race-free binary variable assignment for the states in the flow table by using only three states.
iii) Obtain the modified flow table with an appropriate race-free binary variable assignment for the states. Indicate the binary variable assignment for the states in a transition diagram.

[1x3 Marks]

d) An asynchronous sequential circuit is described by the following excitation and output functions.

$$Y = x_1x_2 + (x_1+x_2)$$

$$Z = y$$

i) Obtain the circuit diagram using logic gates.

[1 Mark]

ii) Derive the transition table and circle the stable states.

[2 Marks]

Q4 a) State the key advantage of Emitter Coupled Logic (ECL) over Transistor-Transistor Logic and briefly explain the reason.

[2 Marks]

b) Give the key reason to select the CMOS logic family over the TTL logic family to implement a circuit.

[2 Marks]

c) State whether the following statements are TRUE or FALSE.

i) TTL input thresholds are typically 0.7 V for a LOW signal and 2.0 V for a HIGH signal.

ii) CMOS technology is based on the use of complementary pairs of MOSFETs, one for pull-up and one for pull-down.

iii) The input voltage thresholds for the CMOS logic are typically around 0.7 V for a LOW signal and 2.0 V for a HIGH signal.

iv) CMOS technology uses only n-type MOSFETs in its circuitry.

[0.5x4 Marks]

d) A digital logic circuit is designed with V_{cc} = 5V, I_{CCH} = 22mA, I_{CCL} = 8mA, V_{OH} = 2.4V, V_{IH} = 2V, V_{OL} = 0.45V, V_{IL} = 0.8V, t_{pHL} = 15nS, t_{pLH} = 22nS, I_{IH} = 40μA and I_{OH} = 5.2mA. Calculate the following performance parameters.

i) Noise margin logic 1 and logic 0.

ii) Power dissipation.

iii) Propagation delay and speed-power product.

iv) Fan-out.

[1x4 Marks]

Q5 a) State whether the following statements are TRUE or FALSE.

i) All IIR filters are non-recursive filters.

ii) The ideal low pass filter cannot be realized in practice.

iii) The roots of the polynomial H(z) are identical to the roots of the polynomial $H(z^{-1})$.

iv) If x(n) is a discrete-time signal, then the value of x(n) at non integer value of 'n' may be defined or not defined; we cannot know until the signal is given.

[0.5x4 Marks]

b) A digital filter is defined by the difference equation;

$$y[n] = 0.99\, y[n-1] + x[n]$$

Is this filter stable? Justify your answer.

[2 Marks]

c) Answer the following questions based on Figure Q5.

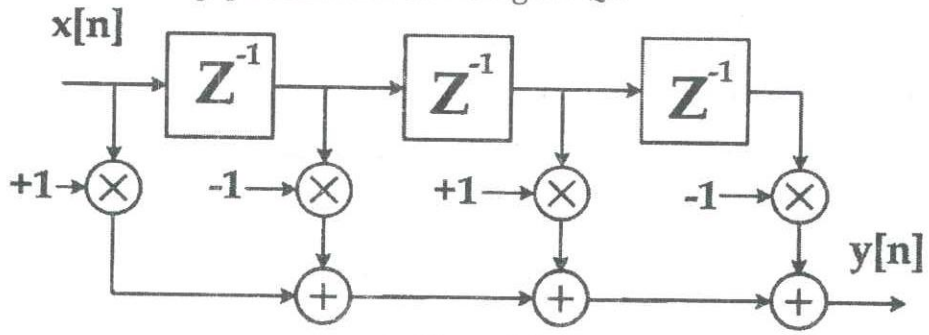

Figure Q5

i) Write the difference equation of the filter.

ii) Calculate the unit step output y[n] for n= -1, 0, 1, 2, 3, 4

[1x2 Marks]

d) Amali implements an FIR filter for a certain application, while Bimal implements an elliptic filter for the same application. Discuss each of their decisions to implement the chosen filters. What is your recommendation to implement between Amali's and Bimal's choices? What factors would influence your decision?

[4 Marks]