UNIVERSITY OF RUHUNA

BACHELOR OF SCIENCE (GENERAL) DEGREE LEVEL II (SEMESTER I)
EXAMINATION- AUGUST 2017

SUBJECT : COMPUTER SCIENCE
COURSE UNIT : COM 2141 (Computer Architecture) DURATION: 1 Hour

*Answer **Two (02)** questions.*

1.

a.

i. Convert 2489.37_{10} to hexadecimal equivalent. Limit your answer to five fractional digits.

ii. Convert $C756A.D_{16}$ to its octal equivalent.

iii. Perform the following binary division. Clearly show the steps you follow.

- $10111011_2 \div 101_2$

iv. Represent -25_{10}, in two's complement notation.

v. Using 8-bit two's-complement notation, solve the mathematical calculation : (-76-59). Explain whether any register overflow exist or not in this operation.

b.

i. "Logic circuit of the full adder can be implemented with the help of two half adder circuits". Explain this statement using a logic circuit of the full adder.

ii. Define an instruction cycle of central processing unit.

iii. Explain three main types of interrupts that would occur while normal processing happens in a processor.

iv. Using a suitable figure, explain how the instruction cycle can be expanded including the interrupt sub cycle.

2.

a.

i. State DeMorgan's theorem in Boolean algebra. Explain two situations where DeMorgan's theorem is applied in Boolean algebra.

ii. Simplify the following expression, by using Boolean algebraic postulates and theorems. Clearly indicate the steps and theorems you apply.

$$(X+Y).(X+Z)+YZ'$$

b.

Assume that you are working for Serkit electronic circuits company. You are asked to develop a LED circuit (Figure 1) to be displayed at a hotel's main entrance with the given output lighting pattern in Figure 2. There are five LED (A, B, C, D, E) lights of red used for the pattern and the LEDs need to be lit in the given pattern with a time delay of 3 seconds. The lighting pattern that need to be shown at each time step is shown in Figure 2. The inputs for the circuit (P,Q,R) is given by a decimal number (0,1,2,3, ….,6) and is input to the combinational circuit as the equivalent binary number of three digits (representation (0_{10} = 000, …. 3_{10}= 011,…, 6_{10} = 110) using the three input terminals (P, Q, R).

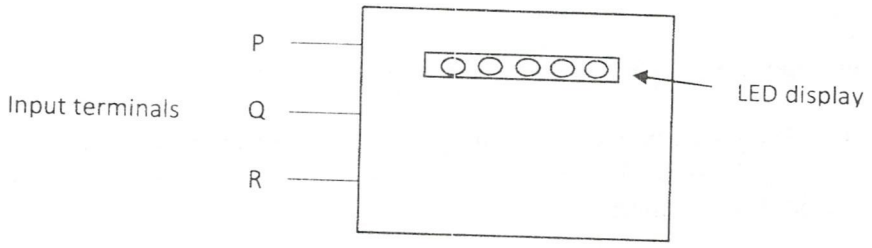

Figure 1

Time	Inputs	The pattern that need to be displayed A B C D E
1s	0	●●○○○
4s	1	○●●○○
7s	2	○○●●○
10s	3	○○○●●
13s	4	○○●●○
16s	5	○●●○○
19s	6	●●○○○

Figure 2

i. Develop a truth table for the inputs (P, Q, R) and outputs (A, B, C, D, and E) of this circuit to display the pattern given in Figure 2.

ii. Express outputs 'A', 'B' and 'C' in sum of products form.

iii. Express the outputs 'D' and 'E' in product of sums form.

iv. Simplify the expression you wrote for 'B' using k-maps.

v. Design a logic circuit to implement the simplified sum–of–products expression for 'B ' obtained in above 2) b) iv) by using **NAND gates**. Clearly indicate the method and steps you follow.

3.

a.

i. List five characteristics of memory systems.

ii. Write down two differences between the random and direct memory access methods.

iii. Write down an equation to calculate the average time to access a specific sector in a hard disk. Give a brief description of each term in your equation.

iv. Compare a DVD and a blue ray disk using three specific facts.

v. "In SR flip flops, the condition S=1, R=1 should be avoided" . Propose a method to overcome this problem. Use a diagram of a logic circuit to explain your answer.

b.

i. Briefly explain the four main instruction types that the CPU can perform.

ii. Write down two advantages of direct addressing mode over indirect addressing mode.

c. Assume that an instruction with two words is stored in memory at addresses 100 and 101. The first word of the instruction specifies the operation code and mode, and the second word specifies the address part. The address field has the value of 200. The content of memory address 200 is 300. The program counter has the value 100 for fetching this instruction. The content of processor register R is 500. The content of memory address 300 is 100.

i. Calculate the effective address for direct and register indirect addressing modes.

ii. Assuming that the indirect addressing mode is used, find the operand value.