UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 4 Examination in Engineering: February 2020

Module Number: ME4310 **Module Name: Analog and Digital Electronics**

[Three Hours]

[Answer **all questions**, each question carries **12 marks**]

Clearly state all assumptions that you may make.
To get full marks, you are supposed to use correct SI units and standard notations in answering.

Q1. a) An Operational Amplifier (Op-Amp) is a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals. The Op-Amp can perform many different operations.

i) Name **four** different operations which an Op-Amp can perform.

ii) Derive equations for the Closed-loop Voltage Gain (A_{cl}) for both inverting and non-inverting amplifier configurations using Op-Amps.

iii) Briefly explain an instance where, an Op-Amp circuit is used as a buffer.

iv) **Figure Q1(a)** shows a closed-loop configured Op-Amp which is having two input voltages. Find out the output voltage (V_{out}) in terms of V_1 and V_2.

[8.0 Marks]

b) In most of the industrial applications, which are operated through sensor feedback signals use 'Voltage to Current Converters' at their front ends.

(i) Define the importance of including Voltage to Current Converters in control systems.

(ii) **Figure Q1(b)** shows a Grounded Load Voltage to Current Converter. Derive an expression for the load current (I_L), in terms of V_{in} and R.

[4.0 Marks]

Q2. a) A filter is a frequency selective circuit that allows to pass only a selected band of desired frequency components from an input signal and attenuates the signals of undesired frequency components. An analog filter operates with the input signals which are continuous on time.

i) Briefly explain the different types of filters, which can be classified by the range of frequencies passed by the filter.

ii) "By using higher order filters, we can increase the sharpness of the filter". Provide valid reasons to support this statement.

Q2 continues to the next page

iii) **Figure Q2(a)** shows an Active Low Pass Filter. Calculate the cut off frequency (f_c) of the circuit.

Note: Assume that the Op-Amp is in its ideal condition.

[7.0 Marks]

b) In the process of filter designing, it is almost impossible to achieve a frequency response of an ideal filter. When designing higher order filters, some ripples are occasionally observed both in the pass band and the stop band. To work on this problem, different filter approximations are used.

i) Compare the behavior of Butterworth and Chebyshev filter approximations using frequency response curves.

ii) By cascading filters, one can design higher order filters. **Figure Q2(b)** shows a 3rd order Butterworth Low Pass filter which is designed by Cascading a 2nd order Sallen-Key Butterworth low pass filter and a 1st order RC low-pass filter. Determine the values for R1, R2, R3, R4 and R5 of this circuit if the cut off frequency to be 2 kHz. (Assume C1=C2=C3=0.1 µF and R1=R2=R5)

Note: The normalised polynomial table for Butterworth filters is provided in **Table Q2(b)**.

[5.0 Marks]

Q3. a) Connecting digital circuitry to sensor devices is simple if the sensor devices are inherently digital themselves. When analog devices are involved, interfacing becomes much more complex. This can be simplified by interfacing analog to digital convertors (ADC) or digital to analog converters (DAC).

i) State three advantages of processing signals in digital domain rather than analog domain.

ii) Briefly explain the importance of following the "Nyquist Sampling Theorem" in the sampling process of analog signals.

iii) Describe the importance of using a "Sample and Hold" circuit in an ADC.

iv) Resolution of an ADC can be defined as the accuracy of quantised values against the actual value of the signal at a given time. Find out the resolution of a 3-bit ADC which is having 10 V Full-Scale Range (FSR).

[8.0 Marks]

b) Most of the Op-Amps which are used today are internally compensated by inserting a compensation capacitor.

i) State the difference of internally compensated and non-compensated Op-Amps, by their frequency response.

ii) Discuss the significance of Amplifier Gain Bandwidth Product (GBP), when designing electronic circuits.

[4.0 Marks]

Q4. A Programmable Logic controller (**PLC**) is a digital electronic device that uses a programmable memory to store instructions and to implement functions such as logic, sequencing, timing, counting and arithmetic in order to control machines and processes.

a) Briefly describe and compare **three** main types of PLCs: unitary, modular and rack-mounted with respect to their capacity, capability, performance, complexity and applications.

[3.0 Marks]

b) A machine having two actuators (A and B) to be equipped with a PLC to perform its function automatically. Each actuator has two sensors so that a sensor signal indicates when they are ON or OFF, and each actuator is operated by a ON or OFF signal. The sequence of two actuators to be performed is: A+ (ON), B+ (ON), A- (OFF), B- (OFF). This sequence must be followed 10 times automatically and any further actuations to be stopped until the process is started manually again. It is required to make sure both actuators are OFF by switching them off when you start the machine manually. A continuous signal should be supplied to actuators each time in order to perform the operation and sensors will detect whether the actuators reach their (+ / ON) or (- / OFF) positions.

i) Produce a flow chart for the complete operation.

ii) Given that the Input and the output address allocation stating from X1 and Y1, and taking START, STOP as push buttons, prepare input and output address allocation table.

iii) Draw a PLC ladder diagram to follow the complete operation above automatically until it stops by pressing the STOP push button or after the usual 10 cycles.

[9.0 Marks]

Q5 a) Use Karnaugh maps to simplify the following expressions.

i) $\bar{A}\,B(\bar{C}\,\bar{D} + \bar{C}\,D) + AB(\bar{C}\,\bar{D} + \bar{C}\,D) + A\,\bar{B}\,\bar{C}\,D$ to a minimum SOP (Sum of Products) form.

ii) $(X + \bar{Y})(W + \bar{Z})(\bar{X} + \bar{Y} + \bar{Z})(W + X + Y + Z)$ to a minimum POS (Product of Sums) form. [2.0 Marks]

b) In a 7-segment display (see **Figure Q5(b)**), relevant segments are to be activated for displaying various digits: 0,1,2,3,4,5,6,7,8 and 9. Using Binary Coded Decimal (BCD) representation for these digits (take A,B,C, and D are the variables), derive an SOP expression for segment "a" using A,B,C, and D. Hence minimize the expression using a Karnaugh map. [4.0 Marks]

c) Derive the truth table and the output wave form for a Gated D Latch and its input wave form shown in Figure Q5(c). Note: You may use the input wave form shown in the figure to derive the output wave form.

[3.0 Marks]

d) The block diagram of a 4x1 MUX is shown in **Figure Q5(d).**

i) Define the function (F) using inputs D_0, D_1, D_2, D_3 and selectors S_0 , S_1.

ii) Derive the Boolean logic expression and design the 4x1 MUX using basic logic gates. [3.0 Marks]

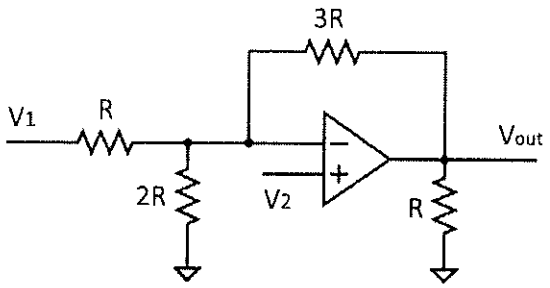


Figure Q1(a): A Closed-loop Configured Op-Amp

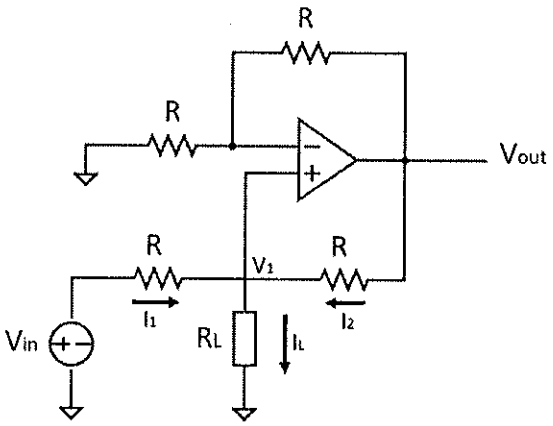


Figure Q1(b): A Ground Load Voltage to Current Converter

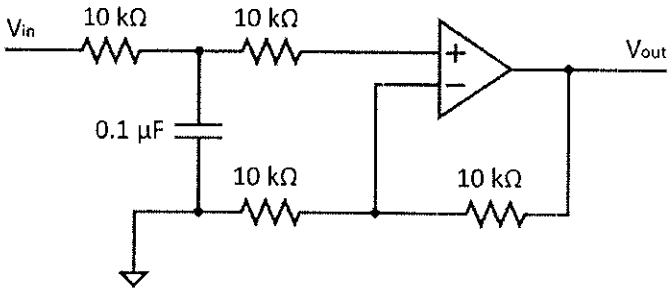


Figure Q2(a): An Active Low Pass Filter

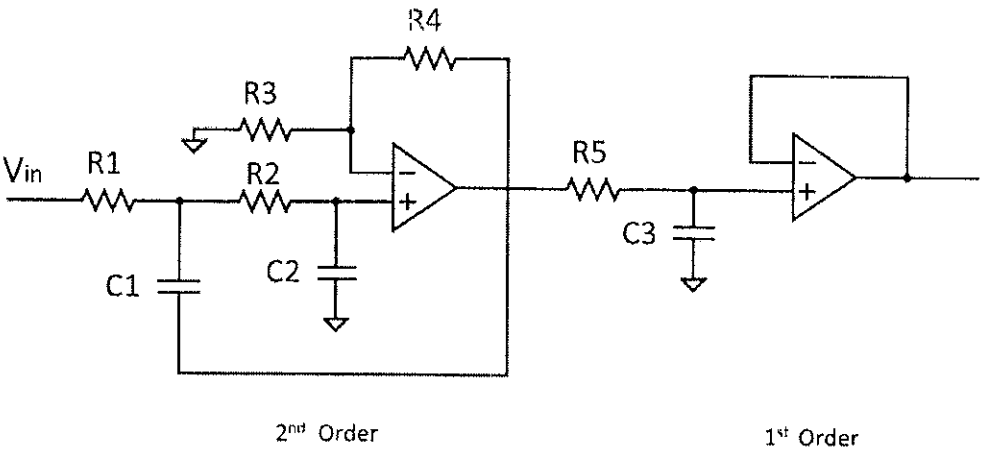


Figure Q2(b): 3rd Order Butterworth Low Pass Filter

Table Q2(b): Normalized Polynomial Table for Butterworth Filters

n	Factors of Polynomial $B_n(s)$
1	$(s+1)$
2	$(s^2+1.4142s+1)$
3	$(s+1)(s^2+s+1)$
4	$(s^2+0.7654s+1)(s^2+1.8478s+1)$
5	$(s+1)(s^2+0.6180s+1)(s^2+1.6180s+1)$
6	$(s^2+0.5176s+1)(s^2+1.4142s+1)(s^2+1.9319s+1)$
7	$(s+1)(s^2+0.4450s+1)(s^2+1.2470s+1)(s^2+1.8019s+1)$
8	$(s^2+0.3902s+1)(s^2+1.1111s+1)(s^2+1.6629s+1)(s^2+1.9616s+1)$

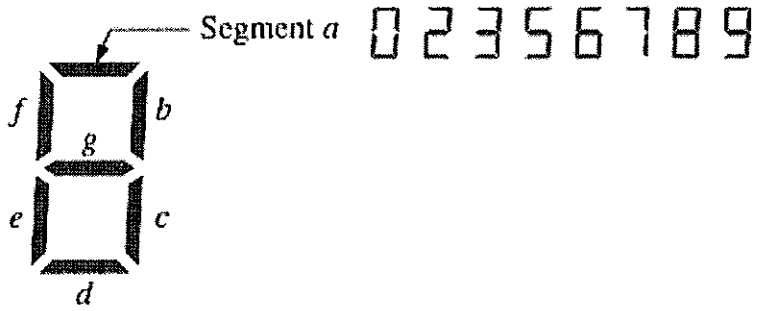
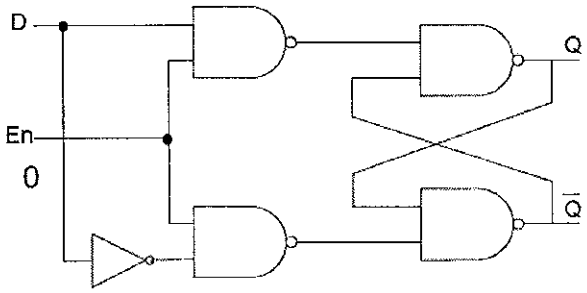


Figure Q5(b): A 7 -Segment Display



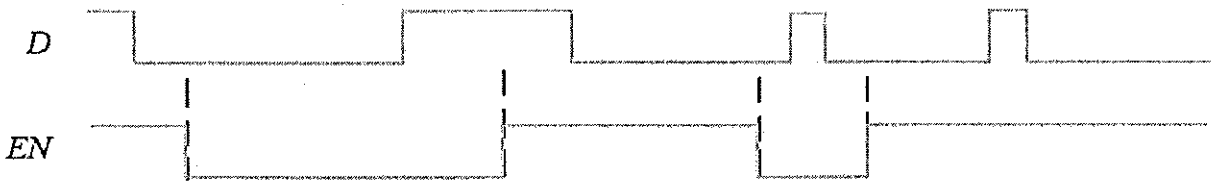


Figure Q5(c): A Gated D Latch

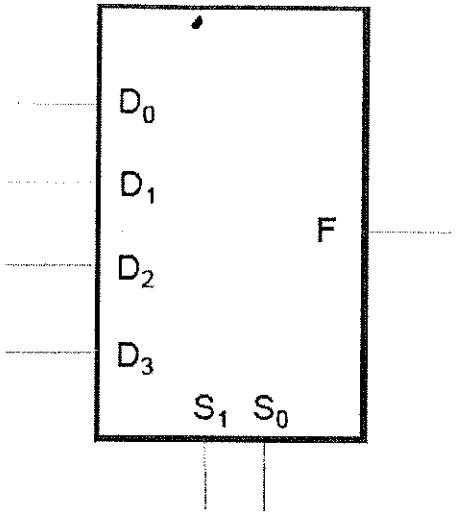


Figure Q5(d): A 4x1 MUX