UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5 Examination in Engineering: August 2018

Module No: EE5201 Module Name: Computer Architecture

[1 hour and 45 minutes]

[Answer all questions. Each question carries 10 marks]

Part II

Q1. a) What is the main difference between user-level threads and kernel-level threads?

[1 Mark]

b) What is the main difference between Uniform Memory Access(UMA) and Nonuniform Memory Access (NUMA) in multiple-processor systems?

[2 Marks]

c) Draw a diagram to show the cache-coherent NUMA (CC-NUMA) organization.

[2 Marks]

d) Describe the following three pipeline hazards that can occur in a instruction pipeline.

i. Resource Hazards

ii. Data Hazards

iii. Control Hazards

[3 Marks]

e) Describe the four categories of user-visible registers.

[2 Marks]

Q2. a) Use the Tow's compliment division to divide 0101 by 0010. Initially the Q register holds the dividend 0101 and A holds 0000. Use the bit shifting and subtraction to find the quotient and the remainder. Show all steps in your answer.

[2 Marks]

b) Describe the difference between the significand underflow and the significand overflow under floating-point arithmetic.

[2 Marks]

c) Describe how RAID 0 can support high data transfer.

[1 Mark]

d) Describe why the solid state drives give low performance when it is more occupied.

[2 Marks]

e) Describe the operating principle of "Aerodynamic gap" head mechanism in magnetic disks.

[2 Marks]

f) What is the reason dynamic RAM requires a refreshing circuitry?

[1 Mark]

Q3. a) List two reasons for the requirement of a memory hierarchy.

[2 Marks]

b) Describe how the data is transferred between the CPU and the Main Memory in a single level cache. Use a diagram in your description.

[2 Marks]

c) What is the advantage of associative mapping compared to direct mapping?

[2 Marks]

d) How the concepts of direct mapping and associative mapping influenced on set-associative mapping?

[2 Marks]

e) In a set-associative mapping cache design, there are 10 sets having 1000 lines each. Find the cache set number of the 778^{th} memory block.

[2 Marks]