UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 2 Examination in Engineering: December 2018

Module Number: EE2202 **Module Name: Introduction to Electronic Engineering**

[Three Hours]

[Answer **all questions,** questions 1, 4 and 5 carries **10 marks,** question 2 carries **13 marks,** question 3 carries **7 marks**]

All notations have the usual meanings.

Q1 a) i) Give the circuit symbols for a NPN transistor and a PNP transistor and name the terminals.

ii) Indicate the directions of all currents.

iii) State the equation relating the currents.

iv) State the biasing rule for normal transistor operation.

[2 Marks]

b) A NPN transistor is in Common-Base configuration.

i) Draw the bias circuit without bias resistors using standard notation.

ii) Give the circuit that defines the reverse saturation current I_{CBO}.

iii) Derive an expression for the DC current gain α.

iv) Sketch the Common-Base input and output characteristics and indicate the saturation, active and cut-off regions.

[3 Marks]

c) A NPN transistor is biased in Common-Emitter configuration.

i) Draw the bias circuit with bias resistors using standard notation.

ii) Derive the equation of the load line.

iii) Sketch the Common-Emitter output characteristics and indicate the saturation, active and cut-off regions.

iv) Plot the load line in the characteristics in part c iii) clearly showing the points and their values where it intercepts the axis.

v) Indicate the points in the load line for the transistor to operate as an inverter.

vi) Modify the circuit in part c) i) for the NPN transistor to operate as an inverter.

vii) Sketch the input and output waveforms for the inverter and state the desired voltage value for the HIGH level of the input.

[5 Marks]

Q2 a) A transistor amplifier with voltage gain A_v, current gain A_i, input resistance r_{in} and output resistance r_o is connected in series with a source of voltage v_s, source resistance r_s and a load R_L.

i) Draw the circuit using the amplifier circuit symbol.
ii) Give an expression for the overall voltage gain v_L/v_s .
iii) Give an expression for the overall current gain i_L/i_s .
iv) State the conditions for a voltage amplifier to operate with overall gain same as the amplifier gain.
v) Express the overall power gain and show that under matched conditions the power gain is given by $A_vA_i/16$.

[3 Marks]

b) i) Draw the AC equivalent circuit for a NPN transistor in Common-Base configuration for emitter resistance r_e and collector resistance r_c.
ii) Draw the Common-Base amplifier circuit and its AC equivalent circuit with the usual notation for the bias resistors and DC sources.
iii) Show that the voltage gain is R_c/r_e where R_c is the collector bias resistor.
iv) If the same transistor is now connected in Common-Emitter configuration, derive values for the input and output resistances.
v) State why the Common-Emitter configuration is better suited for voltage amplification than the Common-Base configuration.
vi) Draw the Common-Emitter transistor amplifier circuit with a source with voltage v_s and source resistance r_s connected to a load R_L.
vii) Draw the AC equivalent circuit for part b) v) and give an expression for the overall voltage gain. [Assume that the amplifier gain is the negative of that in part b) ii)]

[6 Marks]

c) i) Draw the Common-Collector amplifier circuit (with source voltage v_s and source resistance r_s) for open-circuit load and clearly show where the output is taken.
ii) Draw the AC equivalent circuit of part c) i).
iii) Derive an expression for the voltage gain of the amplifier.
iv) For this amplifier show that the power gain Ap is same as the current gain Ai.

[4 Marks]

Q3 a) i) State the meaning of the acronym JFET and give its circuit symbol.
ii) Draw the physical structure of an N-channel JFET (NJFET) and name the terminals.
iii) Sketch the two ways and conditions for forming the depletion regions in the NJFET.
iv) Sketch the drain and transfer characteristics of the NJFET.

[3 Marks]

b) i) State the meaning of the acronym MOSFET.

ii) Draw the physical structure of a Depletion N-type MOSFET (NMOSFET) with normal biasing.

iii) Draw the circuit in part b) ii) with the NMOSFET circuit symbol.

iv) State the condition for operating the NMOSFET in enhancement mode.

v) Sketch the drain characteristics for the NMOSFET operating in depletion and enhancement modes.

[4 Marks]

Q4 a) i) What is a minterm? Write three minterms of a three variable system (A, B, C).

ii) What is a multiplexer in a digital circuit? Draw a schematic to illustrate all the inputs and outputs of a 4 X 1 multiplexer.

iii) Write the truth table of the 4 X 1 multiplexer.

[2 Marks]

b) Reduce the following Boolean expression using Karnaugh Map

i) $F(A,B,C,D) = \sum(0,2,5,7,8,9,10,11,13,15)$

ii) $F(A,B,C,D) = (\bar{A}B + A)(CD + C\bar{D}) + (\overline{A+B} + A\bar{B})(\overline{C\bar{D}} + C)$

[4 Marks]

c) You are asked to design a digital logic circuit with three input variables and two output variables; (A, B, C) and (Z_1, Z_2) respectively. The required specifications are tabulated in Table Q4.

i) Implement Z_1 using only minimum number of NOR gates.

ii) You are given a 4 X 1 multiplexer (1 number), 8 X 1 multiplexer (1 number), and a bank of NOT gates. Implement Z_2 using only required elements.

[4 Marks]

Table Q4 : Truth table of the digital logic circuit

A	B	C	Z_1	Z_2
0	0	0	1	1
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	0	0
1	0	1	0	1
1	1	0	1	1
1	1	1	1	0

Q5 a) i) State the main difference between combinational and sequential logic circuits.

ii) What is meant by state of a sequential logic circuit?

iii) Define a flip-flop (FF) in a sequential logic circuit.

iv) Draw the logic diagram of a JK-FF and write the characteristic table (CT) of the JK–FF.

v) Using the CT of the JK–FF, deduce the CTs of the D-FF and the T-FF.

[5 Marks]

b) You are asked to analyze the digital circuit given in Figure Q5 b). In the circuit, a special clocked MN-FF is used. The MN-FF has two inputs M and N and it operates as follows.

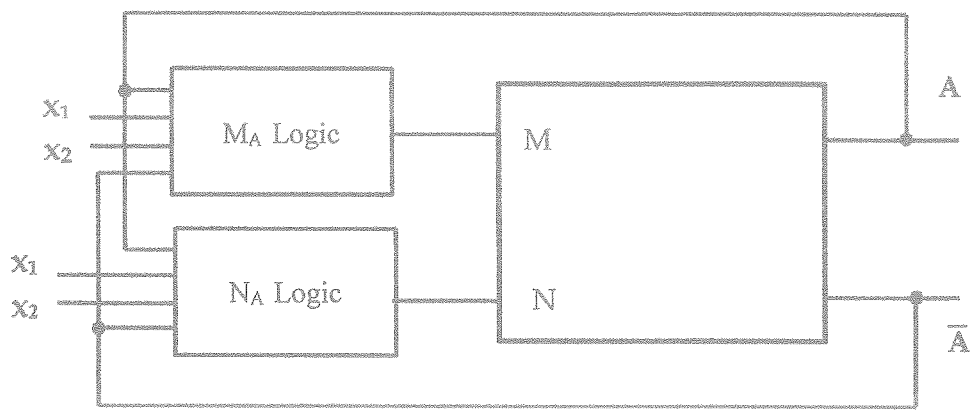

Figure Q5 (b)

- If MN = 00, the next state of the FF output is 1.
- If MN = 01, the next state of the FF output is the same as present.
- If MN = 10, the next state of the FF output is the complement of present.
- If MN = 11, the next state of the FF output is 0.

i) Derive the characteristic table of the MN FF.

ii) The input functions of the FF are given in (1) and (2).

$$M_A = \overline{(x_1 + x_2 + \overline{A}_n)}(x_2 + \overline{A_n}) \qquad (1)$$

$$N_A(A_n, x_1, x_2) = \sum(0,2,3,4,6,7) \qquad (2)$$

Obtain the truth table for the next state of the MN-FF.

Hint: Consider following headings for the truth table.

A_n	X_1	X_2	M_A	N_A	A_{n+1}

Directions: If you have not answered Q5 b)(i) , you may use the JK FF as the MN FF in Q5 b)(ii). Note that then only half of the marks will be given for Q5 b)(ii).

[5 Marks]