UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 4 Examination in Engineering: December 2018

Module Number: EE4302 **Module Name: Digital Electronics**

[Three Hours]

[Answer **all questions**, each question carries 12.5 marks]

Q1 a) i) Define a flip-flop (FF) in a sequential circuit.

ii) In a synchronous sequential logic (SSL) circuit, if there are m different states each with n bits,

I) How many FFs are needed to implement the memory of the SSL?

II) Write an expression to show the relationship between m and n.

iii) Draw a logic diagram to illustrate how a gated SR-FF is modified to form a JK-FF and write the characteristic table of the JK-FF.

iv) Derive the excitation table of the JK-FF.

[4.0 Marks]

b) You are required to design a SSL circuit according to the state diagram illustrated in Figure Q1 using JK FF(s).

i) Obtain the state table (ST) and then use the implication table method to reduce the ST.

ii) Assign states using the binary counting order starting from integer 1.

iii) Derive the excitation table **only** for the input function of the first FF and the output.

iv) Draw complete K'maps for the excitation table derived in part iii).

[6.5 Marks]

c) Draw the **state diagram** of a SSL circuit which detects a serial input sequence of 1001 or thereafter more consecutive 1's. The detection of the required bit pattern can occur in a longer data string and the correct pattern can overlap with another pattern.

[2.0 Marks]

Q2 a) i) Briefly explain the stable states in an asynchronous sequential circuit (ASC)?

ii) What is meant by the fundamental mode of operation of an ASC?

iii) Explain the critical and non-critical race conditions in ASCs.

[2.5 Marks]

b) Consider the reduced flow table given in Table Q2(b). For the states : a=00, b=01, c=11 and d=10,

i) Write the state transitions when the inputs (x_1x_2) change from 11 to 10 and then to 00.

ii) Determine all race conditions and whether they are critical or non-critical.

iii) Obtain a binary state assignment to avoid critical races in the flow table.

[5.0 Marks]

c) Consider the implication table given in Table Q2(c). In the implication table, a to e are the states of the required ASC.

i) Find all compatible pairs.

ii) Find the maximal compatibles by means of a merger diagram.

iii) Find a minimal set of compatibles that covers all the states and is closed.

[5.0 Marks]

Q3 a) i) Name three logic families.

ii) State the meaning of propagation delay and noise immunity for a logic gate.

iii) Explain the operation of a TTL NAND circuit when either or both inputs A and B are low (0 V ≡ logical 0).

[3.5 Marks]

b) i) Figure Q3(b) shows the voltage and current ranges of a TTL NAND gate. Calculate the noise margins of the gate.

ii) For a CMOS NAND gate, the manufacturer has specified the high state and low state currents limits as 0.75 mA and 64 mA, respectively. If the gate has a source current of 40 µA to each driven gate at the high state and the current drawn by the gate is 1.6 mA from each driver gate at the low state, find the high state and low state fan-outs of the gate.

iii) For a CMOS NAND gate, the supply voltage is +12 V. The current drawn by the gate at the high state and the low state are 80 µA and 20 mA, respectively. Calculate the average power dissipation of the gate.

[2.5 Marks]

c) The TTL NAND gate shown in Figure Q3(c) has values of 4 kΩ, 1.5 kΩ, 1 kΩ and 150 Ω for R_1, R_2, R_3 and R_4, respectively. For all the transistors (T_1 -T_4), V_{BE} = 0.7 V and V_{CE}(sat) = 0.2 V, $h_{FE1} = 1$, $h_{FE2} = h_{FE3} = h_{FE4} = 10$. All the diodes are silicon and the collector supply (+V_{CC}) is 12 V.

i) If the load resistance is 5 kΩ, find the high state output voltage.

ii) The output V_0 of the TTL NAND gate (G_0) shown in Figure Q3(c) is connected to the N different inputs (A_1, A_2,.., A_N) of other similar N gates. Express the total collector current in transistor T_4 of G_0 in terms of N at the low state of the gate.

iii) Find the base current (I_B) of transistor T_4 of G_0.

iv) Hence, find the fan-out of the gate at the low state.

[6.5 Marks]

Q4 a) i) What are the main steps involved in analog to digital (A/D) conversion?

ii) Sketch the following discrete sequences.

I $U(n-2)$ II $U(n)-U(n-2)$

III $\delta[n-2]+4\delta[n-3]+2\delta[n-4]$ IV $e^{-n}U(n)$

[2.5 Marks]

b) Determine the output voltage of the D/A converter shown in Figure Q4(b) when the input is 111.

[1.0 Mark]

c) Consider a discrete LTI system with the system equation given in (1), input $x(n)$ and output $y(n)$. Where,

$$y(n+2) - y(n+1) - 2y(n) = x(n+1) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$x(n) = \begin{cases} 3^n & ; n < 0 \\ 2^n & ; n \geq 0 \end{cases}$$

i) Define the Z-transform for the discrete sequence $x(n)$.

ii) What is the relationship between $x(n)$ and $y(n)$ in the time domain and the Z-domain?

iii) Find the output $y(n)$

[5.0 Marks]

d) You are required to design a digital logic circuit which compares or multiplies single bit numbers A_1 and A_2 depending on a control input. When the control input is asserted high, the circuit should work as the comparator and when it is asserted low, it should work as the multiplier. Design the required logic circuit using a suitable multiplexer and the minimum number of logic elements.

[4.0 Marks]

Table Q2(b) : Reduced Flow Table

y_1y_2 \ x_1x_2	00	01	11	10
a	c, –	a, 1	a, 0	d, –
b	d, –	b, 0	a, –	b, 1
c	c, 1	b , –	d, –	c, 0
d	d, 0	c, –	b, -	b, -

Table Q2(c) : Implication Table.

	a	b	c	d	e
b	(a,c) (b,e)				
c	X	(a,e)			
d	(a,c) (d,f)	(e,f)	√		
e	(b,c)	X	(a,c) (b,e)	(a,c) (b,f)	
f	(c,d)	(b,e)	(a,c) (d,f)	X	(b,d)

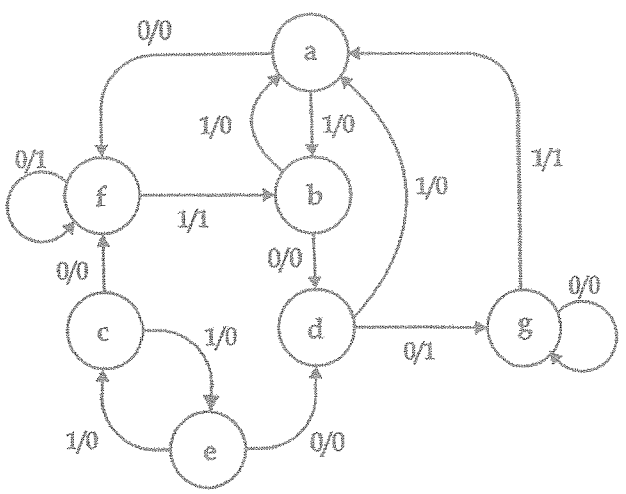

Figure Q1

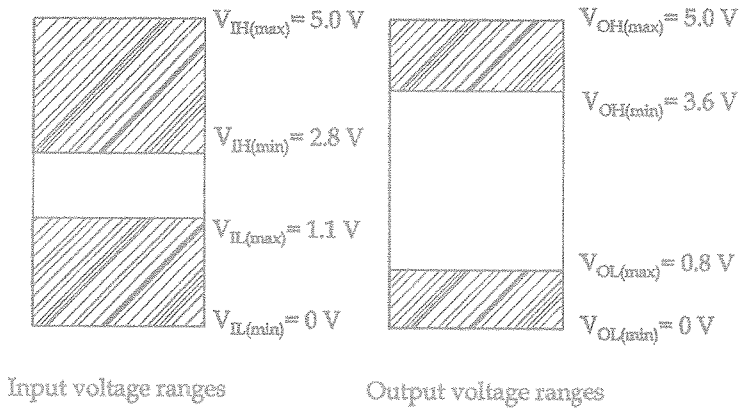

Figure Q3(b)

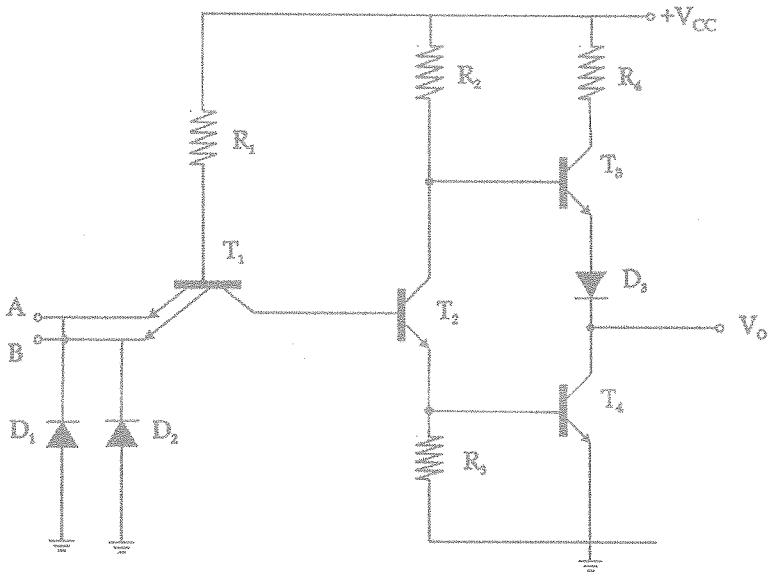

Figure Q3(c)

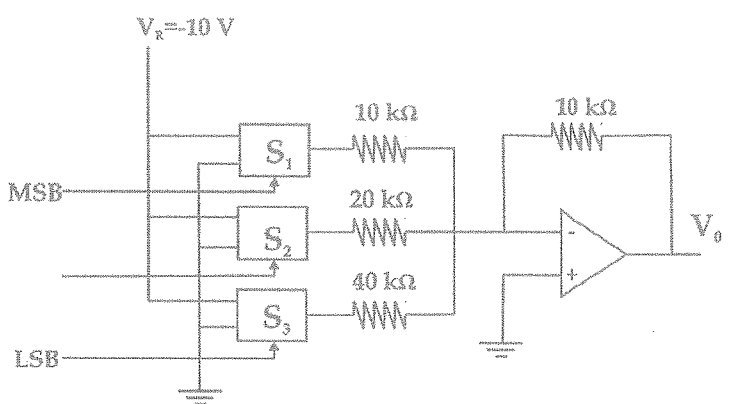

Figure Q4(b): Summing D/A converter Circuit